Panasonic®

PROGRAMMABLE CONTROLLER

FP3/FP10SH
Hardware

FP3/FP10SH Hardware
ARCT1F300E-1 06.9

Matsushita Electric Works, Ltd.

Safety Precautions

Observe the following notices to ensure personal safety or to prevent accidents.
To ensure that you use this product correctly, read this User's Manual thoroughly before use.
Make sure that you fully understand the product and information on safe.
This manual uses two safety flags to indicate different levels of danger.

WARNING

If critical situations that could lead to user's death or serious injury is assumed by mishandling of the product.

-Always take precautions to ensure the overall safety of your system, so that the whole system remains safe in the event of failure of this product or other external factor.
-Do not use this product in areas with inflammable gas. It could lead to an explosion.
-Exposing this product to excessive heat or open flames could cause damage to the lithium battery or other electronic parts.

CAUTION

If critical situations that could lead to user's injury or only property damage is assumed by mishandling of the product.

-To prevent abnormal exothermic heat or smoke generation, use this product at the values less than the maximum of the characteristics and performance that are assure in these specifications.
-Do not dismantle or remodel the product. It could lead to abnormal exothermic heat or smoke generation.
-Do not touch the terminal while turning on electricity. It could lead to an electric shock..
-Use the external devices to function the emergency stop and interlock circuit.
-Connect the wires or connectors securely.
The loose connection might cause abnormal exothermic heat or smoke generation
-Do not allow foreign matters such as liquid, flammable materials, metals to go into the inside of the product. It might cause exothermic heat or smoke generation.
-Do not undertake construction (such as connection and disconnection) while the power supply is on.

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Before You Start

Installation environment

Do not use the FP3/FP10SH unit where it will be exposed to the following:

- **Direct sunlight, and ambient temperatures outside the rang of 0 to 55°C/32 to 131°F.**
- **Ambient humidity outside the range of 30 to 85 % RH and sudden temperature changes causing condensation.**
- **Inflammable or corresive gas.**
- **Excessive vibration or shock.**
- **Excessive airborne dust or metal particles.**
- **Water or oil in any from including spray or mist.**
- **Benzine, paint thinner, alcohol or other organic solvents or strong alkaline solutions such as ammonia or caustic soda.**

Static electricity

- **In dry locations, excessive static electricity can cause problems. Before touching the unit, always touch a grounded piece of metal in order to discharge static electricity.**

Cleaning

- **Do not use thinner based cleaners because they deform the unit and fade the colors.**

Before turning ON the power

When turning ON the power for the first time, be sure to take the precautions given below.

- **Verify that the power supply wiring, I/O wiring, and power supply voltage are all correct.**
- **Sufficiiently tighten the installation screws and terminal screws.**
- **Set the mode selector to PROG. mode.**
- **Remove the dust proofing label, in order to let heat disperse.**
- **Open the cover on the CPU, and connect the connector for the backup battery. The connector is not connected when the CPU is shipped.**

Hardware compatibility between the two models
The FP3 and FP10SH share the same backplane and unit, but the following points should be checked if the type of CPU is changed.

- The internal current consumption varies depending on the CPU. See section 1.3.3, and check the total current consumption.
- With the FP10SH, there are some expansion cables which cannot be used. See section 2.3 to check which cables can be used.
- On the FP3, the programming tool port is an RS422 port (a 15−pin connector), and on the FP10SH, the port is an RS232C port (a 9−pin connector). The cables used for the two ports are different.

Programming tools
When using the NPST−GR software:

- An adapter and cable are required to connect the FP3/FP10SH to a computer (* section 1.5.2).
- With the FP10SH, NPST−GR Ver.4 or a subsequent version is required.

When using the handy−type FP programmer:

- With the FP3, use “FP Programmer II Ver.2 (AFP1114V2).
- The FP programmer cable (AFP5520: 50cm/19.69 in. or AFP5523: 3 m/9.84 ft.) is required to connect the FP3 and the FP programmer II Ver.2.

. **Note**

The FP Programmer II Ver.2 cannot be used with the FP10SH.

Precautions when using the FP10SH
When using the units listed below in combination with the FP10SH CPU, check the version and lot number of the unit.

Type	Order number	Version/Lot number
A/D converter unit G type	AFP3402 AFP3403 AFP3405	The unit can be used if the lot number is 97***** or a subsequent number. (Products manufactured in fiscal 1997 or later)
A/D converter unit I type	AFP3406 AFP3407 AFP3408	
Positioning unit E type	AFP3431E AFP3432E	The unit can be used if the version is Ver. 1.5 or a subsequent version.
Computer communication unit (C.C.U.)	AFP3462	The unit can be used if the version is Ver. 1.2 or a subsequent version.

Before entering a program

Be sure to perform a program clear operation before entering a program.

When using NPST–GR

Procedure:

1. **Press the <CTRL> and <ESC> keys simultaneously to change to the online monitor screen.**
2. **Press the <ESC> key to display the [NPST MENU]. From this menu, select [CLEAR A PROGRAM] from [EDIT A PROGRAM] and press the <ENTER> key.**

```
[CLEAR A PROGRAM]
    CLEAR [ PROG & I/O CMT / PROGRAM / I/O CMT ]
    SELECT WHAT YOU WANT TO CLEAR.
  F1: EXECUTE
```

3. **When [CLEAR A PROGRAM] window appears, press the <F1> key.**

When using FP programmer II Ver.2

Press the keys on the FP programmer II Ver.2, as shown below.

Chapter 1

Features and System Configuration

☞ next page

1.1 General Features

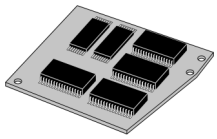
Exclusive RISC (Reduced instruction set computer) processor for high speed processing.

- Basic sequence instructions: 40 ns
- Timer, counter instructions: 280 ns
- Data transfer instructions: 80 ns
- Addition/subtraction instructions: 240 ns

Scan time of 1 ms (for 10 k steps)
The time required for one scan is greatly reduced by paralleling the calculation and transmission processes.

Large program memory with a maximum of 120 k steps
CPU with an internal RAM capacity of 30 k steps. With the addition of the FP10SH optional expansion memory unit of 30 k (or 90 k) steps, a programming capacity of up to 60 k (or 120 k) steps can be obtained.

Expansion memory unit



Transmission port with 115 kbps capability
Greatly increased transmission speed means the program upload and download processing speeds are also greatly increased.

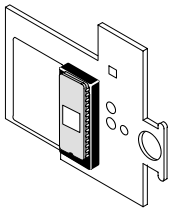
Functions demanded from larger modules are added

- 1 ms unit timer added.
- Real number calculations (trigonometric functions, exponents, logarithms, square roots, etc.)
- Index modifier functions (224 words with bit modifier is also possible)

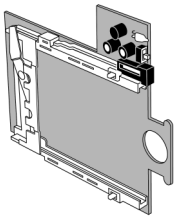
ROM and IC memory card available for optional memory

- Program memory can be converted to ROM (with use of optional ROM operation board).
- Supports the use of IC memory cards for use as program memory or expansion data memory (with use of optional IC memory card board).

ROM operation board



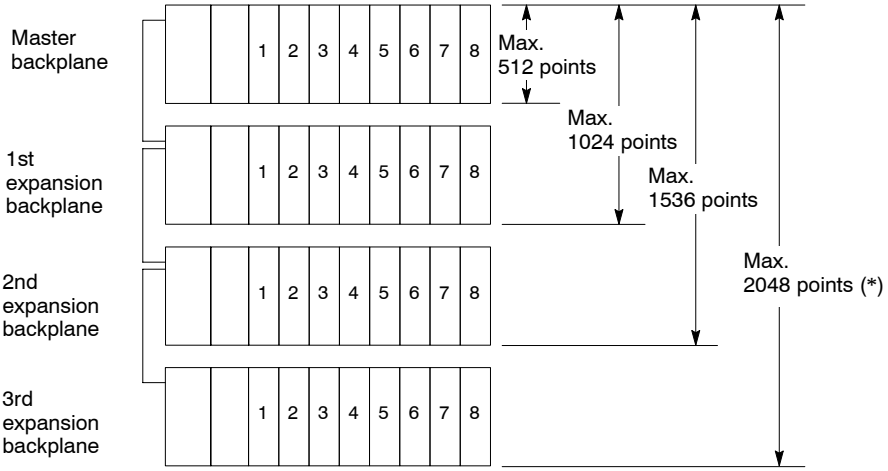
IC memory card board



CPU comes standard with RS232C port

Hardware and software designed with considerations for expansion

With few restrictions when using units in combinations, up to 512 points are possible with an 8–slot master backplane and 64–point units, and this is expandable to up to 1,536 points with additional backplanes (up to 2,048 with the FP10SH). Remodeling and expansion of the equipment is also supported for greater flexibility.



(*) The FP10SH CPU supports expansion of up to 3 expansion backplanes.

Common programming software (NPST–GR software)

Our FP series also supports the same programming software to allow you to make use of the same programs used with the smaller programmable controllers.

Copious selection of units

- Input units (16 points, 32 points, 64 points)
- Output units (16 points, 32 points, 64 points)
- I/O units (3 types)
- Remote I/O-related units (2 types)
- Analog I/O units (7 types)
- Serial data controller units (2 types)
- Positioning control units (4 types)
- Interrupt control unit (1 type)
- Link system-related units (5 types)

Standard modem initialization function

A modem can be connected to the CPU for use with program maintenance systems and remote monitoring and observation systems over normal phone lines.

Expandable over existing networks

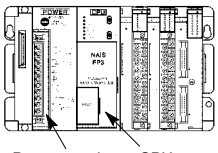
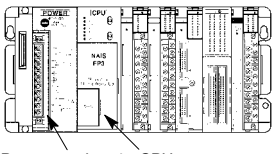
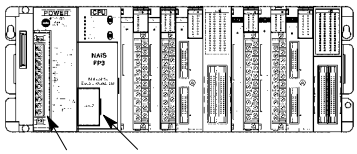
Besides MEWNET–F (remote I/O) systems, the units can be networked between programmable controllers and computers. Units with Ethernet capabilities (ET–LAN units) are also available.

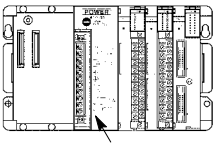
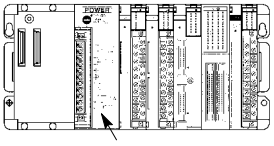
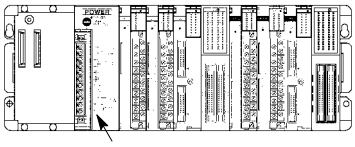
Comparison of processing speed and memory capacity

Item		FP10SH		FP3	
		AFP6221V3	AFP6211V3	AFP3220C–F	AFP3210C–F AFP3211C–F
Processing speed (per an instruction)	Sequence instruction	0.04 μs	0.1 μs	0.5 μs	
	Timer instruction	0.28 μs	0.7 μs	2.0 μs	
	High–level instruction	from 0.08 μs	from 0.2 μs	from dozens of speed μs	
Program capacity		30 k steps (expanded up to 120 k steps)		16 k steps	10 k steps
External input relays (X)		8,192 points		2,048 points	
External output relays (Y)		8,192 points		2,048 points	
Internal relays (R)		14,192 points		1,568 points	
Data registers (DT)		10,240 words		2,048 words	
File registers (FL)		32,765 words		22,525 words to 0 word	
Link relays (L)		10,240 points		1,024 points × 2	
Link data registers (LD)		8,448 words		128 words × 2	

1.2 Basic System Configuration

1.2.1 Basic Configuration and Number of Control I/O Points

Item	Master backplane
3-slot type	 48 I/O points: using three 16-point I/O units 96 I/O points: using three 32-point I/O units 192 I/O points: using three 64-point I/O units
5-slot type	 80 I/O points: using 16-point five I/O units 160 I/O points: using 32-point five I/O units 320 I/O points: using 64-point five I/O units
8-slot type	 128 I/O points: using eight 16-point I/O units 256 I/O points: using eight 32-point I/O units 512 I/O points: using eight 64-point I/O units

Item	Expansion backplane
3-slot type	 48 I/O points: using three 16-point I/O units 96 I/O points: using three 32-point I/O units 192 I/O points: using three 64-point I/O units
5-slot type	 80 I/O points: using five 16-point I/O units 160 I/O points: using five 32-point I/O units 320 I/O points: using five 64-point I/O units
8-slot type	 128 I/O points: using eight 16-point I/O units 256 I/O points: using eight 32-point I/O units 512 I/O points: using eight 64-point I/O units

☞ next page

The I/O units, intelligent units, power supply unit and backplane can be commonly used for the FP3 and the FP10SH.

Although most of the I/O units and intelligent units can be combined freely in the layout, you should check the following points when selecting your units:

- the restrictions on unit types (* section 1.3.2).
- the limitations on current consumption (* section 1.3.3).

The mounting position for the I/O units on each backplane are free and the I/O can be assigned using NPST-GR, so system design and specifications changes are easily supported.

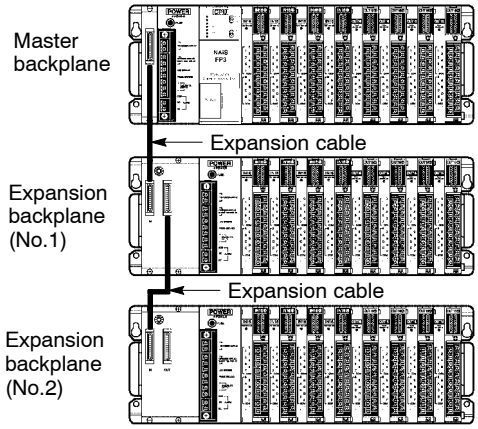
The master and expansion backplanes are available in three types: 3-slot, 5-slot and 8-slot.

The number of I/O points controllable for one backplane for 16–point, 32–point, and 64–point I/O units as shown below.

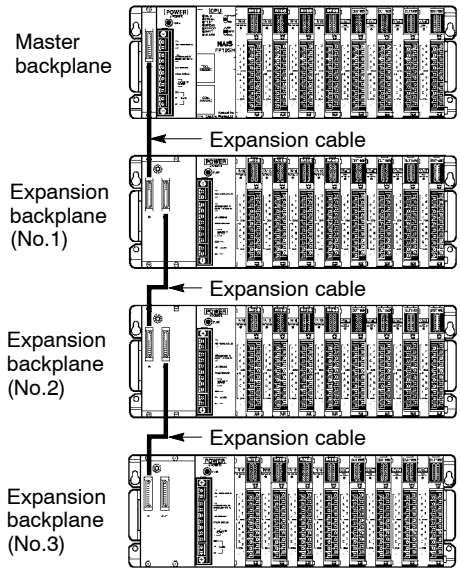
Backplane type	**Using 16–point I/O units**	**Using 32–point I/O units**	**Using 64–point I/O units**
3–slot	48 points	96 points	192 points
5–slot	80 points	160 points	320 points
8–slot	128 points	256 points	512 points

1.2.2 Configuration and Number of Control I/O Points When Expanded

FP3



FP10SH



Both master and expansion backplanes can be connected in any combination between 3–, 5– and 8–slot types.

Up to two (for the FP3) or three (for the FP10SH) expansion backplanes can be connected to a master backplane.
When using 64–point units attached to 8–slot backplanes, up to the following number of points become controllable.

FP3

Master backplane	Expansion backplane	Expansion backplane

512 points + 512 points + 512 points = total 1,536 points

FP10SH

Master backplane	Expansion backplane	Expansion backplane	Expansion backplane

512 points + 512 points + 512 points + 512 points = total 2,048 points

For limitation on expansion of the expansion cable, refer to section 2.3.

Further expansion of I/O points is possible with remote I/O systems.
With remote I/O system, the number of control I/O points can be expanded as shown below.

Type of CPU	When expanded	When using remote I/O system
FP3	Up to 1,536 points	Up to 2,048 points
FP10SH	Up to 2,048 points	Up to 8,192 points

When the I/O equipments are dispersed or when you want to make the control panel compact; use of remote I/O is recommended for I/O point expansion.
The use of expansion backplanes are recommended when the I/O equipments are gathered in a small area or a high response speed is required.

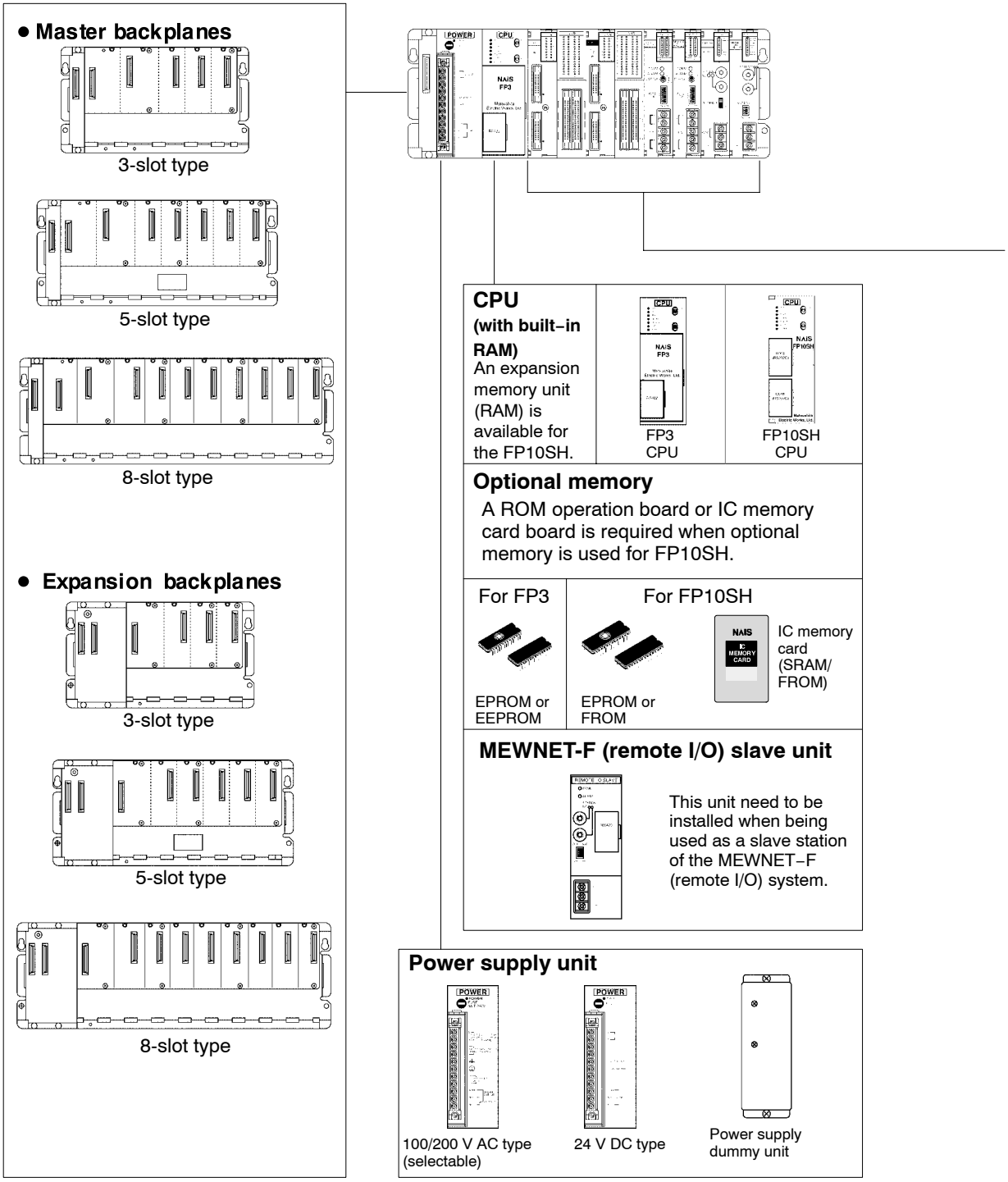
Remote I/O system are available in two types: the MEWNET−F for large−scale network and MEWNET−TR for small−scale network.

☞ **Note**

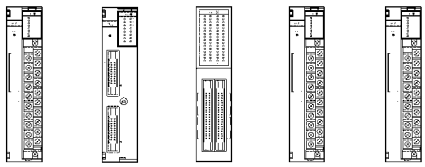
For more information regarding the MEWNET−F and MEWNET−TR, refer to their manuals.

1.3 Unit Combinations

1.3.1 Unit Line–Up

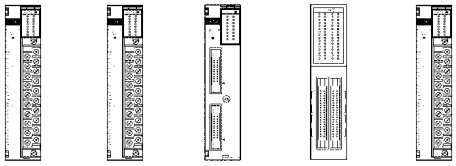


Input units



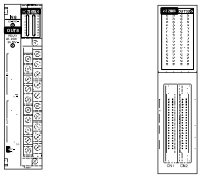
16 points DC type | 32 points DC type | 64 points DC type | 8 points AC type | 16 points AC type

Output units



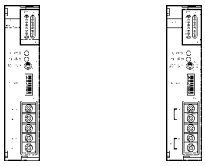
16 points Relay type | 16 points Transistor type | 32 points Transistor type | 64 points Transistor type | 16 point Triac type

I/O mixed units



I:8/O:8, DC input/ Relay type | I:32/O:32, DC input/ Transistor type

Remote I/O-related units

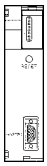


MEWNET-F (remote I/O) master unit | MEWNET-TR master unit

Analog I/O units

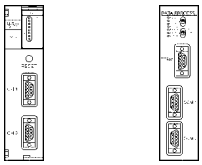
A/D converter unit | D/A converter unit | Thermocouple input unit | RTD input unit

Operation display panel and computer interface unit



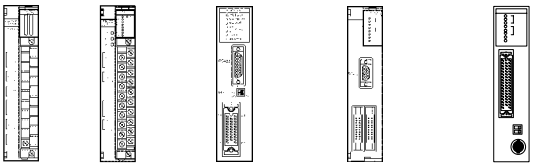
Computer communication unit (C.C.U.)

Serial data controller units



Serial data unit | Data process unit

Position control and motor control units

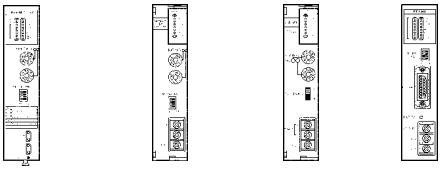


High-speed counter unit | Pulse output unit | Positioning unit E-type | Positioning unit F-type (transistor type) | Positioning unit F-type (Line−driver type)

Interrupt unit

Interrupt unit

Link system-related units



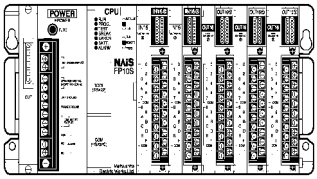
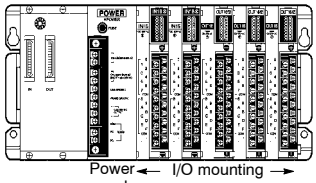
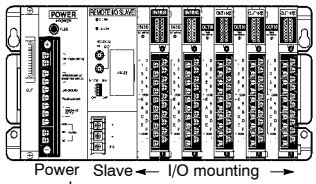
MEWNET-P (optical) link unit | MEWNET-W (wire) link unit | C-NET link unit | ET-LAN link unit

Expansion data memory unit

Expansion data memory unit

1.3.2 Restrictions on Unit Types

Combination of FP3/FP10SH units (A: Available, N/A: Not available)

Set configurations \ Backplanes and units			Master Backplane	Expansion Backplane	Basic Units: Power Supply Unit	Basic Units: CPU	Basic Units: MEWNET−F (remote I/O) Slave Unit
Basic set	 Power supply unit, CPU, I/O mounting area	The most basic configuration for CPU installation. Power supply unit and CPU are installed to a master backplane.	A	N/A	A	A	N/A
Expansion set	 Power supply unit, I/O mounting area	This configuration is to be used for expansion. A power supply unit is installed to an expansion backplane.	N/A	A	A (*)	N/A	N/A
Remote I/O slave station set	 Power supply unit, Slave, I/O mounting area	This configuration is used when the serves as slave station of MEWNET−F (remote I/O system). A power supply unit and remote I/O slave units are installed to a master backplane.	A	N/A	A	N/A	A

☞ Note

(*): A power supply dummy unit may be used to omit the power supply unit (* section 2.7).

Units which can be mounted on I/O mounting area																					
Input Unit	**Output Unit**	**I/O Mixed Unit**	**A/D Converter Unit**	**D/A Converter Unit**	**Thermocouple Input Unit**	**RTD Input Unit**	**Serial Data Unit**	**Data Process Unit**	**High–speed Counter Unit**	**Pulse Output Unit**	**Positioning Unit E type**	**Positioning Unit F type**	**Interrupt Unit**	**MEWNET–TR Master Unit**	**MEWNET–F (Remote I/O) Master Unit**	**MEWNET–W Link Unit**	**MEWNET–P Link Unit**	**ET–LAN Unit**	**C–NET Link Unit**	**C.C.U.**	**Expansion Data Memory Unit**
A	A	A	A	A	A	A	A	A	A *1	A *1	A	A	A	A	A	A *2	A *2	A	A *2	A *2 *3	A
													Up to 2 units		Up to 4 units						
A	A	A	A	A	A	A	A	A	A *1	A *1	A	A	A	A	A	N/A	N/A	N/A	N/A	N/A	A
A	A	A	A *4	A	A	A	A	A	A *5	A *5	A *6	A	N/A	A *7	N/A	N/A	N/A	N/A	N/A	N/A	A

☞ next page

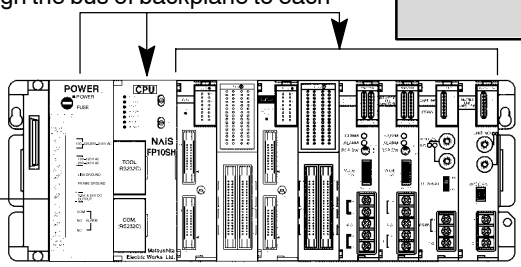
☞ Notes

- **(*1): Interrupt function is available on high−speed counter and pulse output units when the total number of units is 8 or less.**
- **(*2): Up to 3 units in all −MEWNET−W link unit, MEWNET−P link unit, C−NET link unit and computer communication unit (Up to 5 units in all if the CPU is the FP10SH).**
  Up to 2 units in all −MEWNET−W and MEWNET−P− for PC link function.
- **(*3): When using the FP10SH, the computer communication unit Ver. 1.2 or later is required.**
- **(*4): When using the FP10SH, units producted in 1997 or later are required for I and G types (lot No. of 97**** or later).**
- **(*5): The interrupt function is not available when a remote I/O slave unit is connected.**
- **(*6): When using the FP10SH, the positioning unit E−type Ver. 1.5 or later is required.**
- **(*7): When using the FP10SH, the MEWNET−TR transmitter master unit Ver.1.1 or later is required.**

1.3.3 Limitations on Current Consumption

Power supply unit	Rated output current (5 V)
AFP3631	2.4 A
AFP3634	2.4 A
AFP3638	9 A (at ambient temp. 45 °C/113 °F or less) 7 A (at ambient temp. 55 °C/131 °F or less)

Internal power supply (5 V) passes through the bus of backplane to each unit.



Commercial available power supply 24 V

① Power goes from a service power supply to each I/O unit

② Power goes from a commercial available power supply to each I/O unit

Power supply unit	Rated output current (24 V)
AFP3631	0.8 A

Use an external supply power (24 V) from either ① a service power supply or ② commercial available power supply.
Do not connect them (① and ②) in parallel.

Internal supply power (5 V DC)
The 5 V DC power used for driving the internal circuit of each unit is supplied from the power supply unit through the internal bus of the backplane.

External supply power (24 V DC)
The 24 V DC power supply used as the input power supply of the input units and the output circuit driving power of the output units are supplied from the external terminal of each unit.

For 24 V power supply, the service power supply of the power supply unit or a commercial available power supply equipment is used.

Do not connect the service power supply of the power supply unit and the 24 V power supply of commercial available power supply equipment in parallel.

Combination of units

The current consumed by each unit is shown in the following pages.
Give consideration to the combination of units so that the rated capacity of 5 V DC and 24 V DC power supplies should not exceeded.

<Example of current consumption calculation>

The table below shows the combination of typical units on a 8-slot type backplane.

Type	Number of units and backplane used	Current consumption at 5 V DC (mA)	Current consumption at 24 V DC (mA)
FP3 CPU (AFP3211C–F)	**1**	250	–
Master backplane (AFP3502–F)	**1**	100	–
Input unit (32–point) (AFP33024–F)	**2**	240 (120 × 2)	512 (8 × 32 × 2)
Output unit (32–point) (AFP33484–F)	**4**	640 (160 × 4)	384 (3 × 32 × 4)
MEWNET-W link unit (AFP3720)	**1**	350	–
Computer communication unit (AFP3462)	**1**	100	–
FP programmer II Ver.2 (AFP1114V2)	**1**	130	–
Total current consumption		**1,810 mA**	**896 mA**

☞ **Note**

The current consumption at 24 V DC is calculated on the assumption that the number of ON points of input/output unit is at maximum.
The load current for the output units is not included.

Table of current consumption at 5 V DC

Type			Order number	Current consumption at 5 V DC (mA)
FP3 CPU			AFP3210C–F	250
			AFP3211C–F	250
			AFP3220C–F	250
FP10SH CPU			AFP6211V3	700
			AFP6221V3	800
FP10SH optional memory	**Exapnsion memory unit**		AFP6204	30
			AFP6205	30
	ROM operation board		AFP6208	100
	IC memory card board		AFP6209A	100
Master backplane		**3-slot type**	AFP3505–F	100
		5-slot type	AFP3501–F	100
		8-slot type	AFP3502–F	100

☞ next page

Type				Order number	Current consumption at 5 V DC (mA)
Expansion backplane			**3-slot type**	AFP3506–F	100
			5-slot type	AFP3503–F	100
			8-slot type	AFP3504–F	100
Input unit	**DC input**	**16-point, terminal**	**12 to 24 V DC**	AFP33023–F	60
		32-point, connector	**5 V DC**	AFP33014–F	120
			12 to 24 V DC	AFP33024–F	120
		64-point, connector	**12 to 24 V DC**	AFP33027–F	230
				AFP33028–F	230
			24 V DC	AFP33068–F	230
			5 V DC	AFP33017–F	230
	AC input	**8-point, terminal**	**100 to 120 V AC**	AFP33041	60
			200 to 240 V AC	AFP33051	60
		16-point, terminal	**100 to 120 V AC**	AFP33043	60
			200 to 240 V AC	AFP33053	60
Output unit	**Relay output type**	**16-point, terminal**		AFP33203–F	150
				AFP33103–F	150
	Transistor output	**16-point, terminal**	**NPN open collector**	AFP33483–F	100
			PNP open collector	AFP33583–F	120
		32-point, connector	**NPN open collector**	AFP33484–F	160
			PNP open collector	AFP33584–F	160
		64-point connector	**NPN open collector**	AFP33487–F	250
			PNP open collector	AFP33587–F	250
	Triac output	**16-point, terminal**		AFP33703	200
I/O mixed unit	**DC input/relay output type**	**16-point, terminal (I: 8/O:8)**	**12 to 24 V DC**	AFP33223–F	150
	DC input/ transistor output type	**64-point, (I: 32/O:32) connector**	**12 to 24 V DC NPN open collector**	AFP33428–F	230
			12 to 24 V DC PNP open collector	AFP33528–F	230
A/D converter unit	**4-channel, Non-insulated**			AFP3400	500
	G-type (8-channel, non-insulated)			AFP3402	400
				AFP3403	400
				AFP3405	400
	I-type (8-channel, insulated)			AFP3406	400
				AFP3407	400
				AFP3408	400

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1.3 Unit Combinations

Type				Order number	Current consumption at 5 V DC (mA)
D/A converter unit	2-channel (non-insulated)			AFP3410	700
				AFP3411	700
	I-type (insulated)	2-channel		AFP3412	600
				AFP3413	600
				AFP3416	600
				AFP3417	600
		4-channel		AFP3414	1,000
				AFP3415	1,000
				AFP3418	1,000
				AFP3419	1,000
Thermocouple input unit				AFP3420	500
R.T.D. input unit				AFP3421	500
Serial data unit				AFP3460	100
Data process unit				AFP3461	300
High-speed counter unit		1-channel type		AFP3621	150
		2-channel type		AFP3622	220
Pulse output unit				AFP3480	150
Positioning unit E-type		Transistor output type	1-axis type	AFP3431E	250
			2-axis type	AFP3432E	250
Positioning unit F-type		Transistor output type	1-axis type	AFP3431	350
			2-axis type	AFP3432	400
		Line-driver output type	1-axis type	AFP3434	350
			2-axis type	AFP3435	350
			3-axis type	AFP3436	400
Interrupt unit				AFP3452	100
MEWNET-TR master unit				AFP3750	150
MEWNET-F	master unit			AFP3742	450
	slave unit			AFP3743	400
MEWNET-W link unit				AFP3720	350
MEWNET-P link unit				AFP3710	320
ET-LAN link unit				AFP3790	470
C-NET link unit				AFP3463	350
Computer communication unit (C.C.U.)				AFP3462	100
Expansion data memory unit				AFP32091	50
				AFP32092	50
FP programmer II Ver.2				AFP1114V2	130
Teaching unit II				AFP5134	350

Table of current consumption at 24 V DC

Type				Order number	Current consumption at 24 V DC (mA)
Input unit	DC input (12 to 24 V DC)	16-point, terminal		AFP33023–F	8 × n
		32-point, connector		AFP33024–F	8 × n
		64-point, connector		AFP33027–F	6 × n
				AFP33028–F	6 × n
	DC input (24 V DC)	64-point, connector		AFP33068–F	3.5 × n
Output unit	Relay output type	16-point, terminal		AFP33203–F	10 × n
				AFP33103–F	10 × n
	Transistor output	16-point, terminal	NPN open collector	AFP33483–F	6 × n
			PNP open collector	AFP33583–F	6 × n
		32-point, connector	NPN open collector	AFP33484–F	3 × n
			PNP open collector	AFP33584–F	3 × n
		64-point connector	NPN open collector	AFP33487–F	3 × n
			PNP open collector	AFP33587–F	3 × n

☞ Notes

- **"n" expresses the number of inputs or outputs that are ON.**
- **The input unit displays the current flowing to the internal circuit. The other units display the current value required to drive the internal circuit. This value does not include the load current of the output unit.**

Table of output current value of power supply unit

Power supply unit	Order number	Rated output current (mA)	
		at 5 V DC	at 24 V DC
100 V/200 V AC type	AFP3631	2,400	800
	AFP3638	7,000 (* Note 1) 9,000 (* Note 2)	– –
24 V DC type	AFP3634	2,400	–

☞ Notes

- **(*1): At ambient temperature 55 °C/131.0 °F or less**
- **(*2): At ambient temperature 45 °C/113.0 °F or less**

1.4 Expansion System Configuration

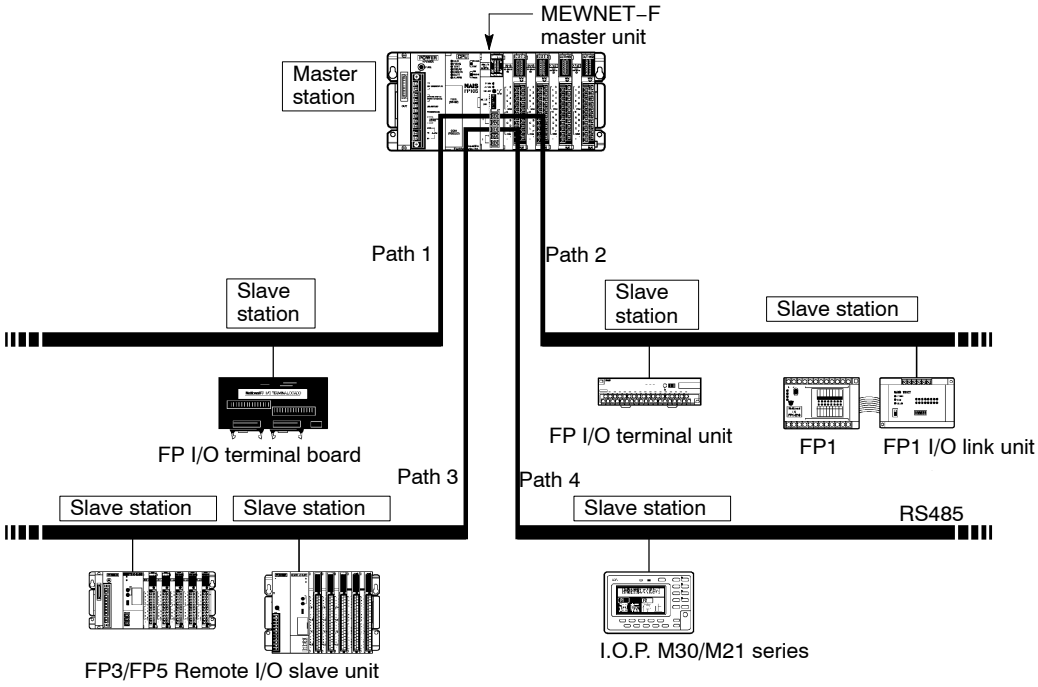
1.4.1 MEWNET−F (remote I/O) Configuration

The MEWNET−F system is a distributed I/O system which uses two−core cable to connect differently located input and output equipments.

The operation box can be installed in one location and used to control I/O equipment in another locations. This system is ideal for network operations when the I/O units are distributed in various places.

The MEWNET−F master unit serve as the master station.

Up to 4 wiring paths from the master station can be arranged to layout of slave stations in a flexible way.
For more information regarding the MEWNET−F configuration, refer to the FP3/FP5 MEWNET−F manual.



Item	Description
Communication method	two-line, half–duplex transmission
Synchronization method	start–stop synchronous system
Communication path	two–core cable (VCTF: 0.75 mm^2 × 2C or twisted–pair cable)
Transmission distance (* Note 1)	total distance: max. 400 m/1,312.34 ft. per port (using VCTF cable) max. 700 m/2,296.59 ft. per port (using twisted–pair cable)
Transmission speed (Baud rate)	0.5 Mbps
Number of slave stations (* Note 2)	max. 32 stations per one master unit
Controllable I/O points	max. 2,048 points per a FP3 CPU max. 8,192 points per a FP10SH CPU
Interface	conforming to RS485
Transmission error check	CRC (Cyclic Redundancy Check) method

☞ **Notes**

- **(*1): When using slave stations with conventional products (AFP87442, AFP3741, and AFP5741) on the same network, the maximum distance for transmissions is 200 m/ 656.168 ft. with VCTF cable and 300 m/984.252 ft. with twisted–pair cable.**
- **(*2): The number of controllable slave stations will differ depending on the type of slave station.**

1.4.2 MEWNET−TR System Configuration

This network system allows control with reduced cabling between the FP3 or FP10SH CPU and input/output units.

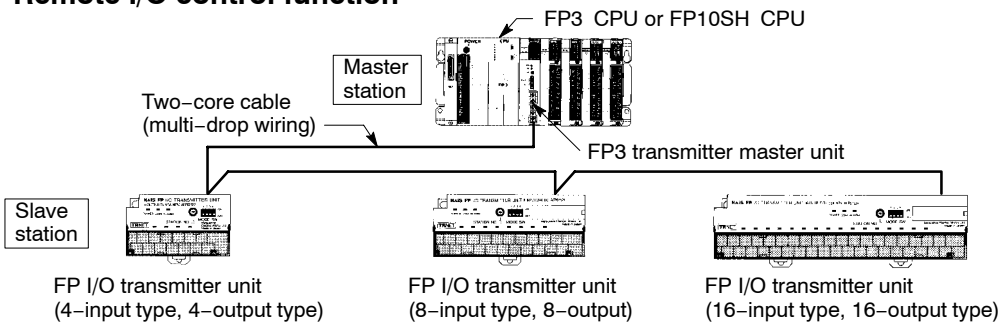
By connecting the exclusive I/O terminal block, you can control the input and output from the I/O terminal block (remote I/O control function).

Allows the connection of two CPUs for the exchange of input/output information (I/O link function).

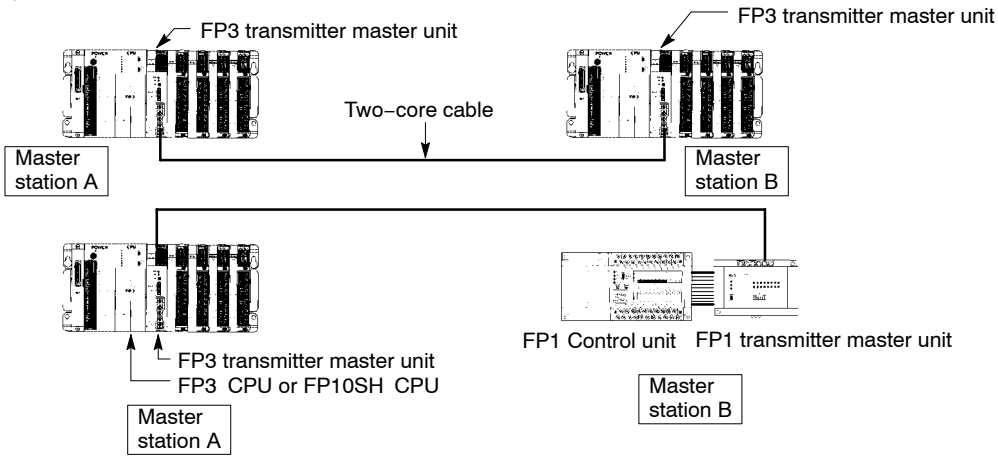
Equipped with a sefety function for selecting the operation status (operation stop mode or operation continue mode) when a communication error occurs.

For more information regarding the MEWNET−TR configuration, refer to the MEWNET−TR manual.

Remote I/O control function



I/O link function



Item	Description
Communication method	two-lines, half–duplex transmission
Synchronization method	start–stop synchronous system
Communication path	two–core cable
Transmission distance	max. 400 m/1,312.34 ft. (using VCTF cable: 0.75mm^2 × 2C) max. 700 m/2,296.59 ft. (using twisted–pair cable)
Transmission speed (Baud rate)	0.5 Mbps
Controllable I/O points	max. 2,048 points per a FP3 CPU max. 8,192 points per a FP10SH CPU
Number of slave stations	max. 32 stations (* Note)
Controllable I/O points	max. 128 inputs and 128 outputs per a master unit
Interface	conforming to RS485
Transmission error check	self–diagnosis data checking method

☞ **Note**

The number of controllable slave stations will differ depending on the type of slave station.

1.4.3 MEWNET−W System Configuration

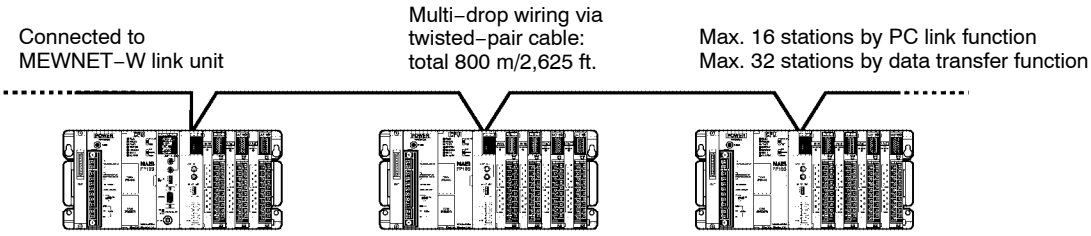
The MEWNET−W system is a link system which enables economical connections between programmable controllers using a twisted−pair cables.

Information can be send and received between programmable controllers in units of bits or words.

Available functions include a PC link function which enables transfer of contact (ON/OFF) and register information, and a data transfer function which selects the source and destination for information transfer using program.

This network is recommended for an economical link between programmable controllers such as an input/output information transfer between devices.

For more information regarding the MEWNET−W system, refer to the MEWNET−W manual.



PC link function

The internal link relays (L) and data link registers (LD) are installed to share data (contact and register information) among the programmable controllers that are connected in an MEWNET network.

Data transfer function

With the **F145 (SEND)**/**P145 (PSEND)** and **F146 (RECV)**/**P146 (PRECV)** instructions to send and receive data, you can specify the format (bit or word) and length of the data to be sent and received, and appoint a destination station or an address. It is easy to share data among the programmable controllers on the network. The remote stations do not need a send/receive program.

Item	Description
Communication method	token bus
Transmission method	baseband transmission
Communication path	twisted−pair cable
Transmission distance	total length: 800 m/2,625 ft.
Transmission speed (Baud rate)	0.5 Mbps
Functions/number of stations	PC link function: max. 16 stations data transfer function: max. 32 stations
PC link capacity per one unit	link relay: 1,024 points link register: 128 words
Other functions	remote programming
Interface	conforming to RS485
R.A.S. function	hardware self-diagnostic function

1.4.4 MEWNET−P Configuration

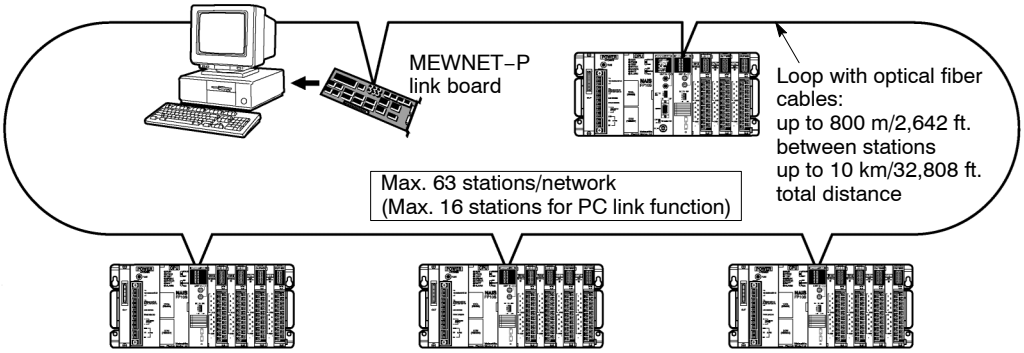
The MEWNET−P (Optical) system links between programmable controllers and between programmable controller and computers with optical fiber cables.

The system provides five functions: PC link, computer link, data transfer, remote programming and computer−to−computer communication functions.

Since it possesses loop−back functions and other RAS functions for measures against malfunctions, observation devices for monitoring the link system are unnecessary. With the use of the optical fiber cables, a highly reliable system with minimal noise interference can be constructed.

This network is recommended for medium−sized computer link system.

For more information regarding the MEWNET−P system, refer to the MEWNET−P manual.



PC link function

The internal link relays (L) and data link registers (LD) are installed to share data (contact and register information) among the programmable controllers that are connected in an MEWNET network.

Computer link function

The host computer sends commands to the programmable controllers on network and writes and reads the input/output information of relays as well as the data register information. The communication programs are unnecessary on the programmable controller side.

Data transfer function

With the **F145 (SEND)**/**P145 (PSEND)** and **F146 (RECV)**/**P146 (PRECV)** instructions to send and receive data, you can specify the format (bit or word) and length of the data to be sent and received, and appoint a destination station or an address. It is easy to share data among the programmable controllers on the network. The remote stations do not need a send/receive program.

Item	Description
Communication method	token ring
Transmission method	baseband transmission
Communication path	two−core optical fiber cable
Transmission distance	between stations: 800 m/2,642 ft. total distance: 10 km/32,808 ft.
Transmission speed (Baud rate)	375 kbps
Functions/number of stations	PC link function: max. 16 stations computer link function: max. 63 stations data transfer function: max. 63 stations
PC link capacity per one unit	link relay: 1,024 points link register: 128 words
Other functions	remote programming computer−to−computer communication
R.A.S. function	loop automatic return function node bypass function self−diagnosis function (hardware and transmission system test)

1.4.5 Computer Link Function

The FP3 can be connected to the computer as an addition to the computer communication unit (C.C.U.). Since a RS232C port comes standard on the CPU for the FP10SH, direct connection to and communication with the computer can be achieved without the addition of any intelligent units.

Using a host computer program, the relay conditions and register contents of the CPU can be read and written.

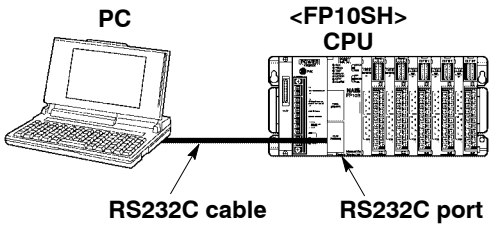
The host computer program are created in BASIC, or other languages, based on the dedicated protocol (MEWTOCOL–COM).

With communications from a host computer, communication programs are unnecessary on the CPU side.

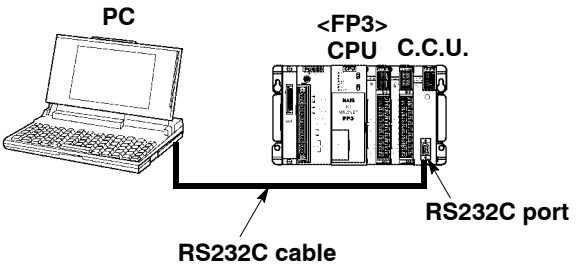
For more information regarding the computer link function, refer to the C–NET link unit manual.

1:1 communication
(One computer to one FP3/FP10SH communication)

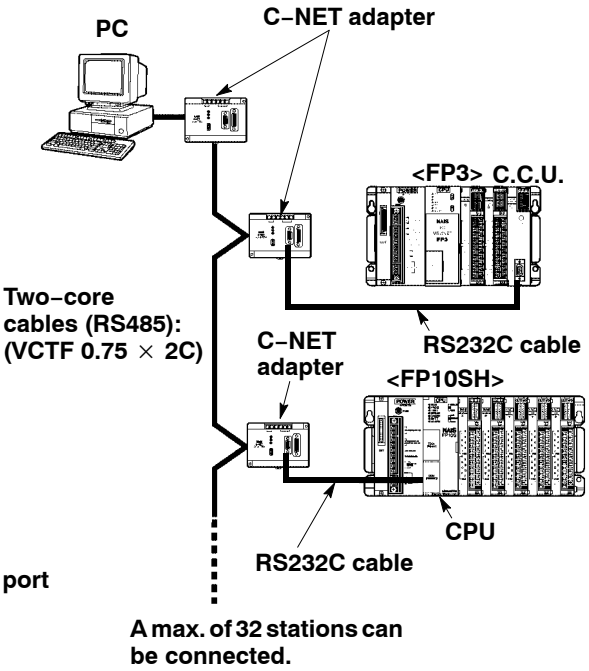
When using the RS232C port of FP10SH CPU



When using the RS232C port of C.C.U.



1:N communication
(One computer to multiple FP3/FP10SH communication)



Item	Description	
	1:1 communication	**1:N communication**
Communication method	full duplex	two wire system, half duplex
Synchronization method	start–stop synchronous system	
Communication path	RS232C cable	two–core cable (VCTF 0.75 mm^2 × 2C)
Transmission distance	max. 15 m/49.2 ft.	max. 1200 m/3,937 ft.
Transmission speed (Baud rate)	300 bps/600 bps/1200 bps/2400 bps/4800 bps/9600 bps/ 19200 bps (* Note 1, 2)	
Transmission code	ASCII	
Transmission format	stop bit: 1 bit/2 bits (* Note 3) parity check: none/even/odd character bits: 7 bits/8 bits	

☞ **Notes**

- **Set the transmission speed, transmission format and unit number with the internal switches of the CPU.**
- **(*1): When using the tool port with 1:N communication with the FP3, the transmission speed is 9,600/19,200 bps.**
- **(*2): With the FP10SH, the transmission speed can be selected from the following: 1,200; 2,400; 4,800; 9,600; 19,200; 38,400; 57,600; and 115,200 bps (however, 38,400 bps and higher can only be used for distances of 3 m/ 9.84 ft. or less).**
- **(*3): When using the tool port with 1:N communication with the FP3, the transmission format is stop bit: 1 bit, odd parity, and character bits of 8 bits.**

1.4.6 Control by MODEM

FP3/FP10SH can be connected to MODEM for programming or computer linking over long distances by using public telephone lines.

When the power supply is turned ON, it will verify whether a MODEM is connected, and, if a MODEM is, it will automatically transmit the AT command to set the MODEM for automatic reception.

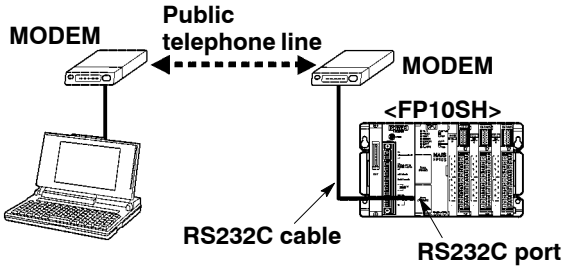
Since the reading and writing of the relay conditions and register contents of the programmable controller can be performed from the host computer, this function is applicable for remote monitoring systems.

When using the tool port, you can use NPST–GR software and perform reading and writing of the programmable controller program and maintenance operations.

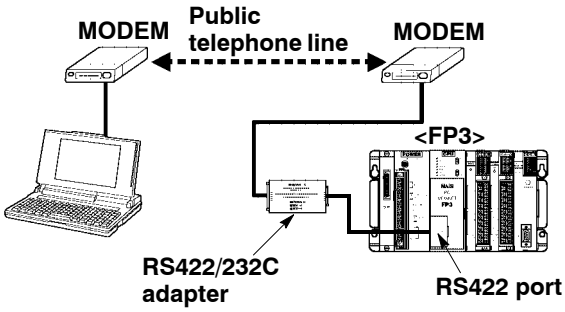
When using the COM port (RS232C), transmission from the programmable controller side can also be programmed.

1:1 communication
Connections to a MODEM can be made using either the RS232C port or the RS422 port.

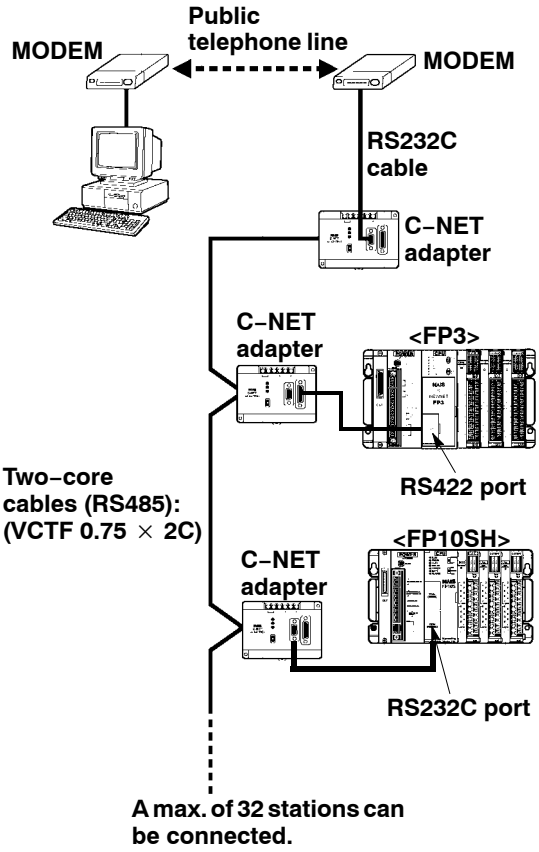
When using FP10SH COM. port (RS232C)



When using FP3 CPU tool port (RS422)



1:N communication
Using the C–NET adapter enables MODEMs to be connected for multiple FP3/FP10SH.



Item	Description	
	FP3	FP10SH
Communication method	half duplex	
Synchronization method	start–stop synchronous system	
Transmission speed (Baud rate) (* Note)	2,400 bps (fixed)	1,200 bps/2,400 bps/ 4,800 bps/9,600 bps/ 19,200 bps/38,400 bps/ 57,600 bps/115,200 bps
Transmission code	ASCII	
Transmission format (total: 10 bits) (* Note)	Start bit: 1-bit	
	Stop bit: 1-bit/2-bit	
	Parity check: none/odd/even	
	Character bit: 7-bit/8-bit	

☞ **Note**

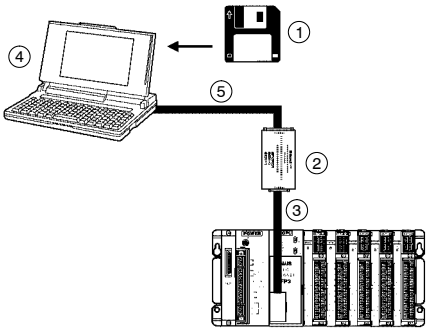
Set the transmission speed and transmission format using the internal switches of the CPU.

1.5 Programming Tools

1.5.1 Tools Needed for Programming

1.5.1.1 Using NPST–GR Software for FP3

Necessary tools



① **NPST–GR software**
This is a program editing and debugging software package that can be used with all programmable controllers in the FP series.

② **RS422/232C adapter** (AFP8550)
Adapter needed for connection between the FP3 CPU and the computer.

③ **FP PC cable**
Cable needed for connection between the tool port (RS422) of FP3 CPU and connector of RS422/232C adapter.
AFP5520 (50 cm/19.69 in.)
AFP5523 (3 m/9.84 ft.)

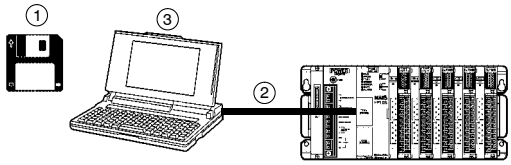
For the following, use commercially available products.

④ **Commercially available PC**
(IBM PC–AT or 100 % compatible machine)

⑤ **Commercially available RS232C cable**

1.5.1.2 Using NPST–GR Software for FP10SH

Necessary tools



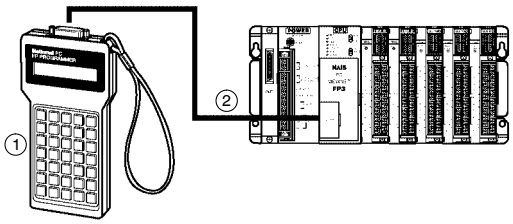
① **NPST–GR software**
This is a program editing and debugging software package that can be used with all programmable controllers in the FP series.

② **FP PC cable** (AFB85853)
Cable needed for connection between the FP10SH CPU and the computer.

③ **Commercially available PC**
(IBM PC–AT or 100 % compatible machine)

1.5.1.3 Using FP Programmer II Ver.2 for FP3 Only

Necessary tools



① **FP Programmer II Ver.2**
Handheld programming device (AFP1114V2)

② **FP peripheral cable**
Cable needed for connection between the FP3 and the FP programmer II.
AFP5520 (50 cm/19.69 in.)
AFP5523 (3 m/9.84 ft.)

☞ **Note**

The FP programmer II Ver.2 does not support functions exclusive for FP10SH, such as operands and instructions newly added to the FP10SH. Therefore, we recommend you use NPST-GR software Ver.4 for controlling FP10SH.

1.5.2 Table of Programming Tools

Type		Description	Order number
PC software	**NPST-GR software Ver. 4**	Program editing software for use with commercially available computers. (System required: IBM PC-AT or 100 % compatible with 800 KB or more free EMS, 4 MB or more hard disk space, MS-DOS Ver. 6.2 or later, and EGA or VGA display mode)	AFP266541
	FP PC cable for FP10SH	Cable needed for connection between the tool port (RS232C) of FP10SH CPU and 9 pins connector of computer (IBM PC/AT or 100% compatible).	AFB85853 (3 m/9.84 ft.)
	FP PC cable for FP3	Cable needed for connection between the tool port (RS422) of FP3 CPU and 15 pins connector of RS422/232C adapter.	AFP5520 (50 cm/ 19.69 in.) AFP5523 (3 m/9.84 ft.)
	RS422/232C adapter	Adapter needed for connection between the FP3 CPU and the computer.	AFP8550
Programmer	**FP programmer II Ver. 2**	Handheld programming device for FP3.	AFP1114V2
	FP peripheral cable	Cable needed for connection between the tool port of FP3 and the FP programmer II's communication port.	AFP5520 (50 cm/ 19.69 in.) AFP5523 (3 m/9.84 ft.)

☞ **Note**

When connecting to a computer (IBM PC/AT or 100% compatible), use a commercially available 9–pin/25–pin adapter.

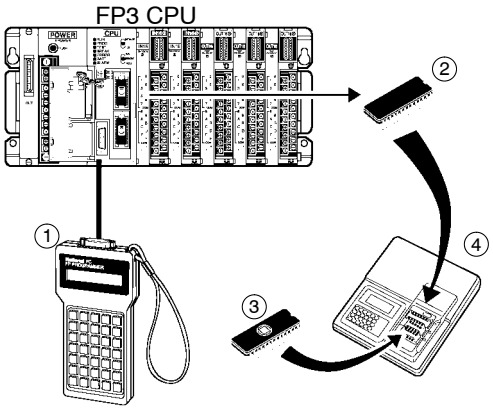
1.5.3 Tools Needed for ROM Writing of FP3

The memory (AFP5202) is an EPROM, and is used to store programs and carry out ROM operations. A commercially available ROM writer is necessary in order to write data.

The master memory (AFP5206) is an EEPROM, and is used to copy programs. When installed in the FP3 CPU, the contents of the internal RAM of the FP3 CPU (supported by FP3 CPU Ver. 4.4 or later) can be copied.

1.5.3.1 When Creating a ROM With a Commercially Available ROM Writer, Through a Master Memory (EEPROM)

Necessary tools



① **FP programmer II Ver.2 and FP peripheral cable** (* section 1.5.1.3)

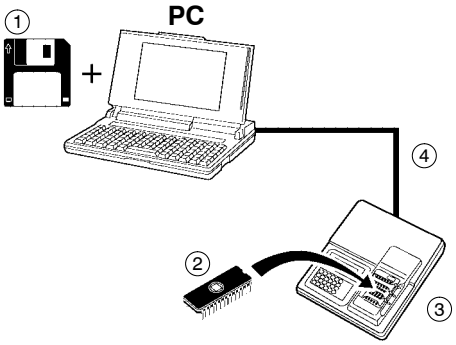
② **Master memory** (AFP5206)
(μPD28C256CZ−20, X28C256PI−20 or equivalent)

③ **Memory** (AFP5202)
(M5M27C256AK−12 or equivalent)

④ **Commercially available ROM writer**
A ROM writer that can be used with memory ② or ③ (27C256 or 28C256 type).

1.5.3.2 When Creating a ROM With NPST–GR Software and a Commercially Available ROM Writer

Necessary tools



① **PC and NPST–GR software** (* section 1.5.1.1)

② **Memory** (AFP5202)
(M5M27C256AK–12 or equivalent)

③ **Commercially available ROM writer**
A ROM writer that can be used with memory ② (27C256 type).

④ **Commercially available centronics cable or commercially available RS232C cable**
Use a cable that conforms with the specifications of the ROM writer.

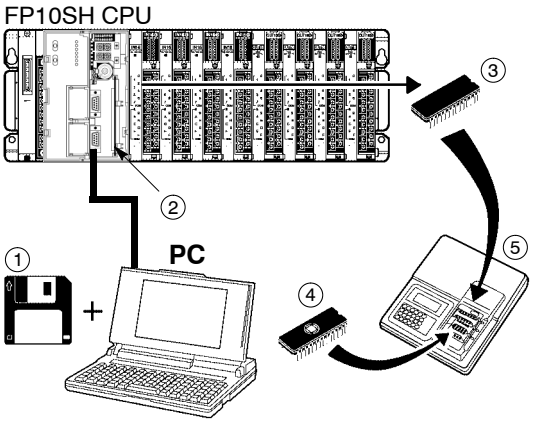
1.5.4 Tools Needed for ROM Writing of FP10SH

The memory (AFP5209) is an EPROM, and is used to store programs and carry out ROM operations. A commercially available ROM writer is necessary in order to write data.

The master memory (AFP5208) is a FROM, and is used to copy programs. When installed in the FP10SH CPU, the contents of the internal RAM of the FP10SH CPU (supported by FP10SH CPU Ver.2 or later) can be copied.

1.5.4.1 When Creating a ROM With a Commercially Available ROM Writer, Through a Master Memory (FROM)

Necessary tools



① **PC, NPST–GR software and cable** (* section 1.5.1.2)

② **ROM operation board** (AFP6208)

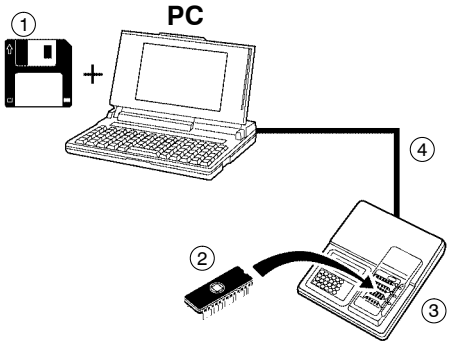
③ **Master memory** (AFP5208)
(SST–29EE020–150–4C–PH or equivalent)

④ **Memory** (AFP5209)
(M27C2001–150F1 or equivalent)

⑤ **Commercially available ROM writer**
A ROM writer that can be used with memory ④ (27C2001 type).

1.5.4.2 When Creating a ROM With NPST–GR Software and a Commercially Available ROM Writer

Necessary tools



① **PC and NPST–GR software** (* section 1.5.1.2)

② **Memory** (AFP5209)
(M27C2001–150F1 or equivalent)

③ **Commercially available ROM writer**
A ROM writer that can be used with memory ② (27C2001 type).

④ **Commercially available centronics cable or commercially available RS232C cable**
Use a cable that conforms with the specifications of the ROM writer.

Chapter 2

Parts and Its Specifications

☞ next page

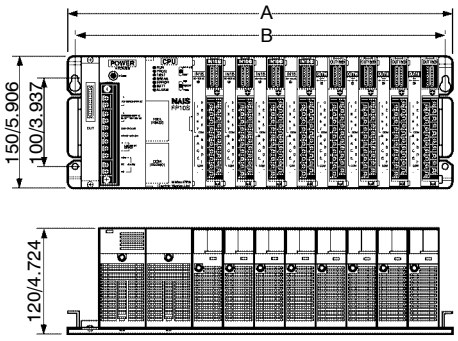
2.1 Specifications

2.1.1 FP3/FP10SH General Specifications

Item	Descriptions
Ambient temperature	0 to 55 °C/32 to 131 °F
Storage temperature	–20 to +70 °C/–4 to +158 °F
Ambient humidity	30 to 85 % RH (non-condensing)
Storage humidity	30 to 85 % RH (non-condensing)
Breakdown voltage	1,500 V AC for 1 minute between AC external terminal and frame ground terminal 500 V AC for 1 minute between DC external terminal and frame ground terminal
Insulation resistance	100 MΩ or more (measured with a 500 V DC megger testing) between external terminal and frame ground terminal
Vibration resistance	10 to 55 Hz, 1 cycle/min: double amplitude of 0.75 mm/ 0.030 in., 10 min on 3 axes
Shock resistance	98 m/s^2 or more, 4 times on 3 axes
Noise immunity	1,500 Vp-p with pulse widths 50 ns and 1 μs (based on in-house measurements)
Operating conditions	Free from corrosive gases and excessive dust

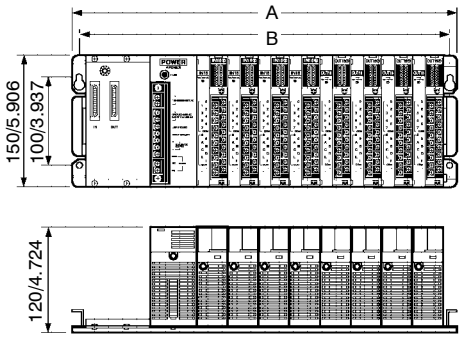
2.1.2 Dimensions

Master backplane



(unit: mm/in.)

Expansion backplane



(unit: mm/in.)

Type	A (mm/in.): Overall length	B (mm/in.): Mounting hole pitch
3-slot type	260/10.236	245/9.646
5-slot type	330/12.992	315/12.402
8-slot type	435/17.126	420/16.535

2.1.3 FP3 Performance Specifications

Item		Descriptions		
Order number		**AFP3210C–F**	**AFP3211C–F**	**AFP3220C–F**
Program method		relay symbol		
Control method		cyclic operation		
Controll–able I/O points	**using one backplane**	max. 512 points		
	using master and two expansion backplanes	max. 1,536 points		
	using remote I/O system	max. 2,048 points		
Program memory	**built-in memory**	RAM		
	optional memory	EPROM/EEPROM		
Program capacity (* Note 1)		max. 9,727 steps		max. 15,871 steps
Number of instruc–tions	**basic**	83 types		
	high-level	237 types	241 types	241 types
Operation speed (typical value)	**basic instructions**	from 0.5 μs per instruction		
	high–level instructions	varies from 10 μs to 100 μs		
Relays	**external input relays (X)**	2,048 points		
	external output relays (Y) (* Note 2)	2,048 points		
	internal relays (R) (* Note 3)	1,568 points		
	timer/counter (C) (* Note 3)	total 256 points (The numbers of timer (T) and counter (C) can be changed.) down type ON-delay timer: 0.01 to 327.67 s, 0.1 to 3276.7 s or 1 to 32767 s down type preset counter: 1 to 32,767 counts		
	link relays (L) (* Note 2, 3)	1,024 points × 2 roots (2 PC links)		

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Item		Descriptions		
Order number		**AFP3210C−F**	**AFP3211C−F**	**AFP3220C−F**
Memory areas	**data registers (DT) (* Note 3)**	2,048 words		
	File registers (FL) (* Note 1, 3)	0 to 8,192 words		8,192 to 22,525 words
	link data registers (LD) (* Note 3, 4)	128 words × 2 roots (2 PC links)		
	timer/counter set value area (SV)	256 words		
	timer/counter elapsed value area (EV)	256 words		
	index registers (IX, IY)	2 words		
Differential points (DF and DF/)		unlimited number of points		
Auxiliary timer		unlimited number of points, down type timer (0.01 to 327.67 s)		
Master control relay points (MCR)		64 points		
Number of labels (JP and LOOP)		256 labels		
Number of step ladder (* Note 3)		1,000 stages		
Number of subroutine		100 subroutines		
Number of interrupt program		25 programs		
Comment input function (* Note 5)		not available	available	not available
Sampling trace function (* Note 6)		not available	available	available
Clock/calendar function		year, month, day, hour, minute, second and day of week		
Link functions		PC link, computer link, data transfer, remote programming and MODEM capability		
Self-diagnostic function		watching dog timer, memory malfunction detection, I/O malfunction detection, backup battery malfunction detection, program syntax check, etc.		
Other functions		program edition during RUN **(* Note 7)**, forced ON/OFF, interrupt input, test run, constant scan and machine language program option		
Memory backup time (lithium battery storage time)		AFP3210C−F : min. 17,000 hours (typical value : approx. 34,000 hours) AFP3211C−F, AFP3220C−F : min. 10,000 hours (typical value : approx. 22,000 hours)		

☞ next page

☞ Notes

- **(*1): The capacity will differ depending on the system register settings.**
- **(*2): Can also be used as an internal relay.**
- **(*3): Hold or non–hold type can be set.**
- **(*4): Can also be used as a data register.**
- **(*5): Max. 2,730 points. Up to 12 characters per 1 comment.**
- **(*6): Can perform sampling up to a maximum of 1,000 samples (4,000 words) for data of 16 contacts and 3 words.**
- **(*7): During the ladder symbol input of NPST–GR, program edits during RUN cannot be performed.**

2.1.4 FP10SH Performance Specifications

Item		Descriptions	
Order number		**AFP6221V3**	**AFP6211V3**
Program method		relay symbol	
Control method		cyclic operation	
Controll–able I/O points	**using one backplane**	max. 512 points	
	using master and three expansion backplanes	max. 2,048 points	
	using remote I/O system	max. 8,192 points	
Program memory	**built-in memory**	RAM	
	Optional memory	IC memory card **(* Note 4)** or EPROM/FROM **(* Note 5)**	
Program capacity		approx. 30 k steps (Approx. 60 k or 120 k steps available by installing optional expansion memory.)	
Number of instruc–tions	**basic**	95 types	
	high-level	431 types	
Operation speed (typical value)	**basic instructions**	from 40 ns per instruction	from 100 ns per instruction
	high–level instructions	from 80 ns per instruction	from 200 ns per instruction
Relays	**external input relays (X)**	8,192 points	
	external output relays (Y) (* Note 1)	8,192 points	
	internal relays (R) (* Note 2)	14,192 points	
	timer/counter (* Note 2)	total 3,072 points (TM number of timer (T) and counter (C) can be changed.) – down type ON-delay timer: 0.001 to 32.767 s, 0.01 to 327.67 s, 0.1 to 3276.7 s or 1 to 32,767 s – down type preset counter: 1 to 32,767 counts	
	link relays (L) (* Note 1, 2)	10,240 points	
	pulse relays (P) (* Note 1, 2)	2,048 points	
	alarm relays (E) (* Note 1, 2)	2,048 points	

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Item		Descriptions	
Order number		**AFP6221V3**	**AFP6211V3**
Memory areas	**data registers (DT) (* Note 2)**	10,240 words	
	file registers (FL) (* Note 2)	32,765 words	
	link data registers (LD) (* Note 2, 3)	8,448 words	
	timer/counter set value area (SV)	3,072 words	
	timer/counter elapsed value area (EV)	3,072 words	
	index registers (I)	14 words (I0 to ID) (with bank switching, 224 words portions can be used)	
Differential points (DF and DF/)		unlimited number of points	
Auxiliary timer		unlimited number of points, down type timer (0.01 to 327.67 s)	
Master control relay points (MCR)		256 points (when using the 90 k step expansion memory, up to a total of 512 points can be used for the no. 1 and 2 programs)	
Number of labels (JP and LOOP)		256 points (when using the 90 k step expansion memory, up to a total of 512 points can be used for the no. 1 and 2 programs)	
Number of step ladder (* Note 2)		1,000 steps (can only be used for the no. 1 program)	
Number of subroutine		100 subroutines (can only be used for the no. 1 program)	
Number of interrupt program		25 program (can only be used for the no. 1 program)	
Comment input function		available (either the IC memory card board or ROM operation board are required)	
Sampling trace function		max. 1,000 samples (16 contacts and 3 words/sample)	
Clock/calendar function		year, month, day, hour, minute, second and day of week	
Link functions		PC link, computer link, data transfer, remote programming and MODEM capability	
Self-diagnostic function		watching dog timer, memory malfunction detection, I/O malfunction detection, backup battery malfunction detection, program syntax check, etc.	
Other functions		program edition during RUN, forced ON/OFF, interrupt input, test run and constant scan	
Memory backup time (lithium battery storage time)	**CPU only**	min. 4,800 hours (typical : approx. 29,000 hours)	min. 9,500 hours (typical : approx. 57,000 hours)
	when used expansion memory	min. 4,300 hours **(* Note 6)** (typical : approx. 25,000 hours)	min. 7,600 hours **(* Note 6)** (typical : approx. 44,000 hours)

☞ next page

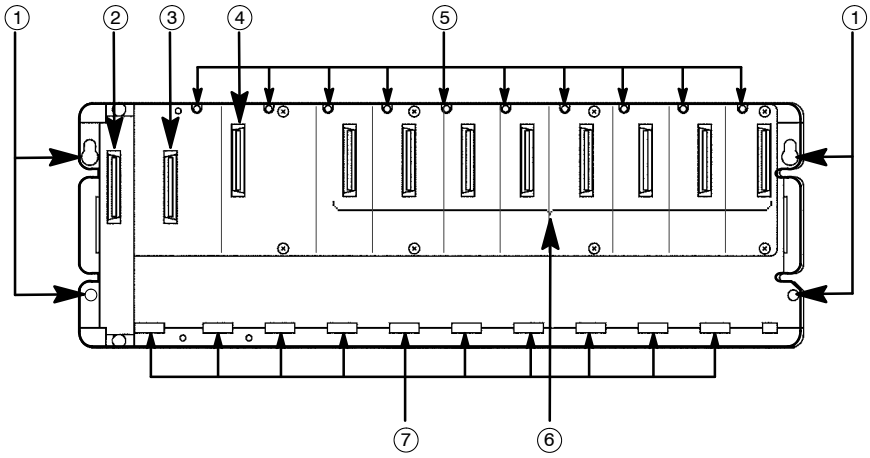
☞ Notes

- **(*1): Can also be used as an internal relay.**
- **(*2): Hold or non–hold type can be set.**
- **(*3): Can also be used as a data register.**
- **(*4): In addition to the IC memory card, the IC memory card board (AFP6209A) is required.**
- **(*5): In addition to the ROM, the ROM operation board (AFP6208) is required.**
- **(*6): The value when the 90 k steps type expansion memory board (AFP6205) is used.**

2.2 Backplane for FP3/FP10SH

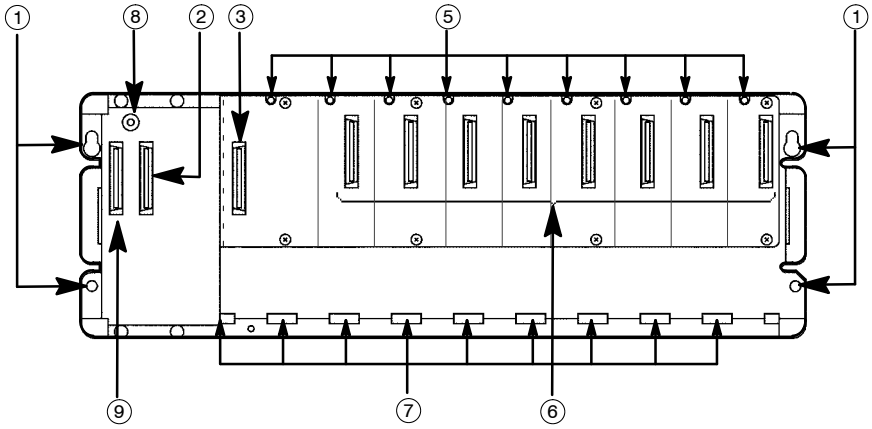
Master backplane

Illustration: 8–slot type



Expansion backplane

Illustration: 8–slot type



Parts Terminology and Functions

① **Backplane mounting holes**
for mounting the backplane to the control panel. Use M5 screw for the mounting.

② **Connector for expansion cable (OUT)**
for more details regarding the cable connecting, refer to section 4.1.3.

③ **Connector for power supply unit**

④ **Connector for CPU**

⑤ **Unit installation holes**
for installing the unit to the backplane. Use the screw supplied with the unit for installation.

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⑥ **Connector for various units**
Use the supplied covers to cover the slots where no unit is attached.

⑦ **Unit guide holes**
Align the tab on the unit with this hole when installing the unit to the backplane.

⑧ **Board number set switch**
set the board number for the expansion backplane.
The I/O address will be allocated in the order of the board number (* section 4.1.1.1).

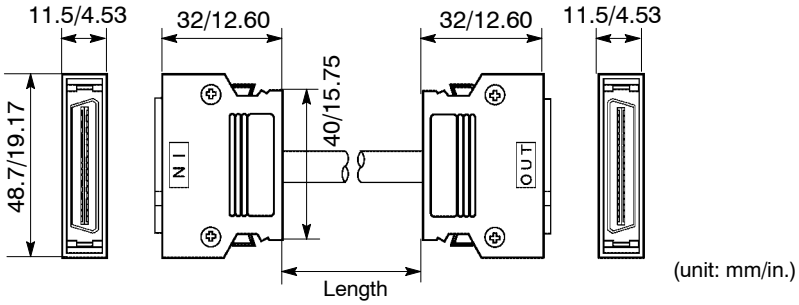
⑨ **Connector for expansion cable (IN)**
connect an expansion cable when using an expansion backplane. When not using one, do not remove the covers on the connectors.

Type of Backplane

Type		Number of slot	Order number	Weight
Master backplane	**3-slot type**	3	AFP3505–F	approx. 700 g/24.692 oz.
	5-slot type	5	AFP3501–F	approx. 900 g/31.747 oz.
	8-slot type	8	AFP3502–F	approx. 1,200 g/42.329 oz.
Expansion backplane	**3-slot type**	3	AFP3506–F	approx. 700 g/24.692 oz.
	5-slot type	5	AFP3503–F	approx. 900 g/31.747 oz.
	8-slot type	8	AFP3504–F	approx. 1,200 g/42.329 oz.

2.3 Expansion Cable

Dimensions



Type of Expansion Cable

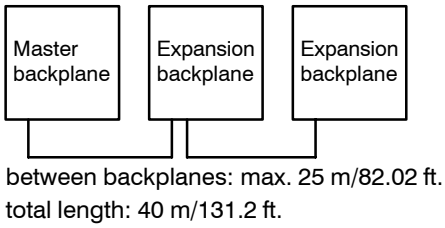
Length	Order number	Weight
0.5 m/1.6 ft.	AFP3510	approx. 110 g/3.880 oz.
1 m/3.3 ft.	AFP3511	approx. 170 g/5.996 oz.
3 m/9.8 ft.	AFP3513	approx. 370 g/13.051 oz.
10 m/32.8 ft.	AFP35110	approx. 1,100 g/38.802 oz.
15 m/49.2 ft.	AFP35115	approx. 1,700 g/59.966 oz.
25 m/82.0 ft.	AFP35125	approx. 2,700 g/95.241 oz.

Limitation on expansion

Be aware that the usable expansion cables will differ depending on the type of CPU being used.

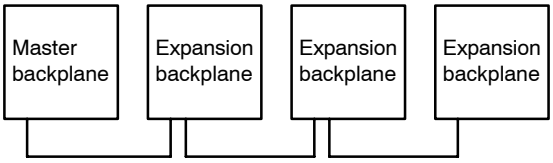
FP3

- Up to two expansion backplanes can be added.
- The use of expansion cable is limited as shown below.



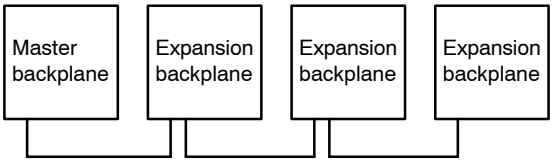
FP10SH

- Up to three expansion backplanes can be added.
- The expansion cable of length “25 m/82.0 ft.” cannot be used.
- The use of expansion cable is limited as shown below in the standard setting (at the time of shipment).



between backplanes: max. 3 m/9.8 ft.
total length: 9 m/29.5 ft.

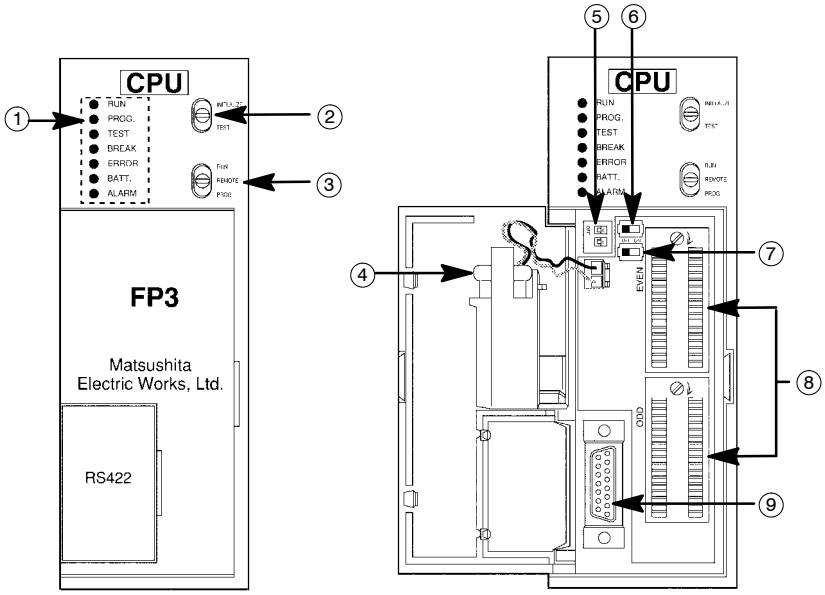
- To further extend the distance between backplanes, set system register 444 to “K1: long mode.”



between backplanes: max. 15 m/49.2 ft.
total length: 30 m/98.43 ft.

2.4 FP3 CPU and Optional Memory

2.4.1 FP3 CPU



Parts Terminology and Functions

① **Status indicator LEDs**
display the operating condition and error statuses (* section 2.4.1.1).

② **Initialize/test switch**
is used to clear the errors, initializes the operation memory and set the test operation mode (* section 2.4.1.2).

③ **Mode selector**
is used to change the operation mode (* section 2.4.1.3).

④ **Backup battery**
for backup of the internal memory (RAM). Not connected when the instrument is delivered.

⑤ **Memory protect and baud rate selector**
is used to select the writing operation for the program memory and to set the baud rate for the tool port.

Switch number	Item	Switch position	
		ON	OFF
1	Program memory protection switch	Write protected	Write enabled
2	Baud rate selector for tool port	9600 bps	19200 bps

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⑥ **Memory selector**
selects either the RAM or the ROM as the program memory.

RAM  **ROM**

⑦ **Device (ROM type) selector**
switches the type of ROM being used between EPROM (memory) and EEPROM (master memory).
The device (ROM type) selector is only on Ver. 4.4 or later FP3 CPU.

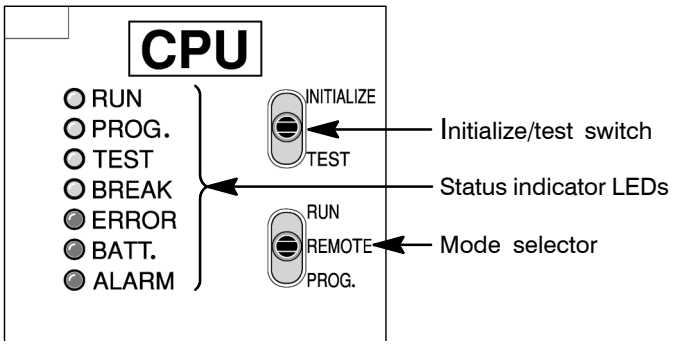
EPROM  **EEPROM**

⑧ **Optional ROM sockets**
is used to install an optional EPROM or EEPROM memory. The upper socket is for even−numbered address ROM (EVEN) and the lower socket is for the odd−numbered address ROM (ODD).

⑨ **Tool port** (RS422)
is used to connect a programming tool.

Weight

Type	Weight
FP3 CPU	approx. 350 g/12.346 oz.



2.4.1.1 Status Indicator LEDs

These LEDs display the current mode of operation or the occurrence of error.

LED	Description
RUN (green)	This lights in the RUN mode, to indicate that the program is being executed. It flashes during forced input/output.
PROG. (green)	This lights in the PROG. mode. Operation stops while this LED is lighted. It flashes when waiting for connection of a distributed slave station. If the memory is initialized, the brightness dims, indicating that initialization is being executed.
TEST (green)	This lights in the test mode.
BREAK (green)	This lights in the operation halts at a break during a test run or halts during the step operation mode for the test run.
ERROR (red)	This lights if an error is detected during the self–diagnostic function.
BATT. (red)	This lights when the voltage of the backup battery drops below a specific value.
ALARM (red)	This lights if a hardware error occurs, or if operation slows because of the program, and the watchdog timer is activated.

2.4.1.2 Initialize/Test Switch

This switch clears errors, initializes the memory, and sets the test operation mode. The setting of mode selector is relevant when initializing the CPU memory.

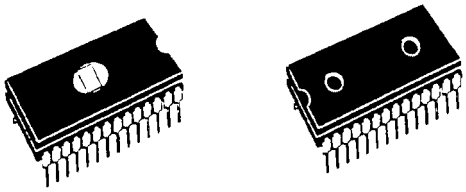
Switch position	Operation mode
INITIALIZE (upward)	**In the PROG. mode:** The contents of the operation memory are initialized. However, the system register (including the I/O map) and the program are not initialized. If a self−diagnostic error code of 42 or lower is occured, the special internal relays R9000 to R9008 and the special data register DT9000 are not cleared. **In the RUN mode:** Operation errors, remote I/O system errors, and battery errors are cleared.
(center)	The switch should normally be left in this position.
TEST (downward)	Setting this switch to the downward position in the PROG. mode, accesses the test mode. Switching to the RUN mode in this state, initiates test operation. To return from the test mode to the normal operation, return this switch to the center position in the PROG. mode.

2.4.1.3 Mode Selector

Use the mode selector to start and stop the operation of the FP3 CPU. For test operations, set the initialize/test switch to TEST position.

Selector position	Operation mode
RUN (upward)	This sets the RUN mode. The program is executed, and operation begins.
REMOTE (center)	This enables operation to be started and stopped from a programming tool. At the stage where the selector is changed, when switching from the PROG. to the REMOTE mode, the system remains in the PROG. mode, and when switching from the RUN to the REMOTE mode, it remains in the RUN mode.
PROG. (downward)	This sets the PROG. mode. In this mode, programming can be done using tools, the test mode can be accessed, and the operation memory can be initialized using the Initialize/tset switch.

2.4.2 Memory (EPROM) and Master Memory (EEPROM)



The FP3 can be operated using only the installed built−in RAM, but use of commercially available EPROM/EEPROM is also possible if necessary.

The memory (EPROM) should be used for program storage and ROM operation, and the master memory (EEPROM) should be used for copying and transferring programs. (EEPROM is supported by Ver. 4.4 or later FP3 CPU.)

With the FP3, two memories are used as a pair, an even−numbered address ROM (EVEN) and an odd−numbered address ROM (ODD).

Type of FP3 optional memories

Type	Memory (EPROM)	Master memory (EEPROM)
Using I.C.	M5M27C256AK−12 or equivalent	μPD28C256CZ−20 or equivalent
Order number	AFP5202 (2 pieces in a set)	AFP5206 (for 16 k steps) (2 pieces in a set)
Writing method	Commercially available ROM programmer	You can write program to EEPROM installing it on the CPU. (A ROM programmer is not required.)
Use	Suitable for program storage or ROM operation.	Suitable for copying and transmitting the master program (I/O comments are not written to ROM)

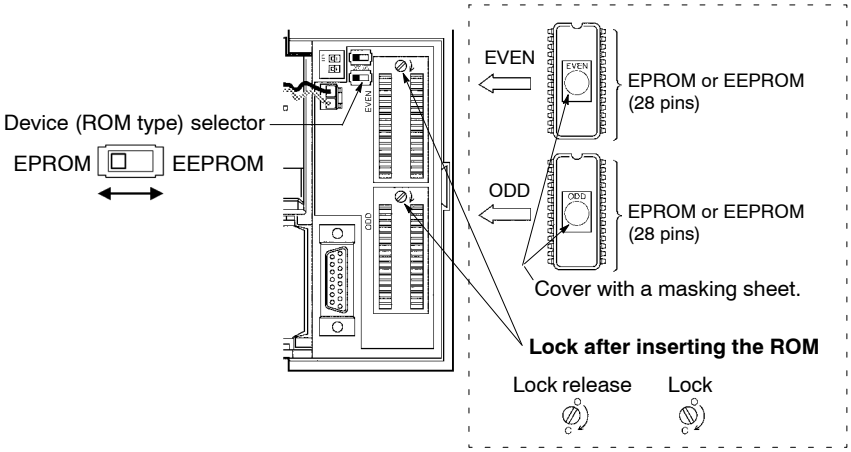
Contents written to ROM

The contents of program and system registers are written to the memory or master memory. Consequently, when the ROM is operated, the contents of the program are rewritten at the same time as those of the system registers.

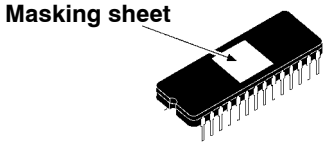
Be aware that the contents of operation memories such as internal relays and data registers are not written to the memory or mastaer memory.

☞ Notes

- **When installing or removing the EPROM or EEPROM, always make sure the power supply to the CPU has been turned OFF first.**
- **Set the device (ROM type) selector to either “EPROM” or “EEPROM”, depending on which type of ROM is being used.**
- **Carefully adjust the pitch of the memory IC leads to the width of the leads for the IC socket and securely insert the optional memories in the correct direction for the grooves.**



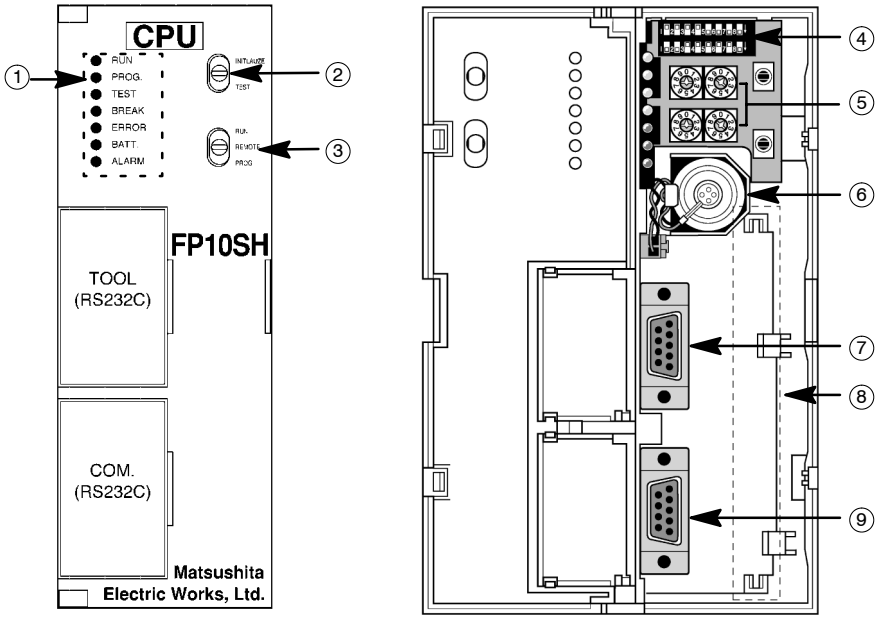
- **With the FP3, two memories are used as a pair, an even−numbered ROM (EVEN) and an odd−numbered ROM (ODD). When installing the ROM, check carefully to make sure it is installed facing the correct direction.**
- **When removing the ROM from the IC socket, use of an IC EXTRACTOR is recommended. Note that the surface of the IC socket might be damaged by using a screwdriver.**
- **Always attach the masking sheet to cover the window on the memory (EPROM). If the masking sheet is not attached, flashes and other light sources may cause misoperation.**



- **Always make sure the divice (ROM type) selector matches the type of memory. If the wrong setting is entered, runaway operation or malfunction could occur.**
- **The device (ROM type) selsctor should be set with the power supply turned OFF. The setting changes as soon as the power supply is turned ON.**

2.5 FP10SH CPU and Optional Memory

2.5.1 FP10SH CPU



① **Status indicator LEDs**
display the operating condition and error statuses (* section 2.5.1.1).

② **Initialize/test switch**
is used to clear the errors, initializes the operation memory and set the test operation mode (* section 2.5.1.2).

③ **Mode selector**
is used to change the operation mode (* section 2.5.1.3).

④ **Operation condition switches**
are used to set the baud rate of the programming tool, to select the program memory, to select the writing operation for the program memory, and to set the transmission format for the COM port (* section 2.5.1.4).

⑤ **Station number setting switches**
are used to set the station numbers (UNIT No.) for the computer link function of the tool port and the COM port (* section 2.5.1.5).

⑥ **Backup battery**
for backup of the internal memory (RAM). Not connected when the instrument is delivered.

☞ next page

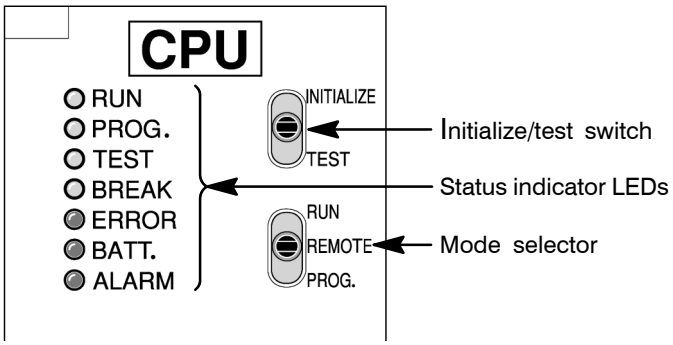
⑦ **Tool port (RS232C)**
is used to connect a programming tool.

⑧ **Option slot**
is used when installing an optional IC memory card board or a ROM operation board.

⑨ **COM port (RS232C)**
is used to connect a computer or other devices with RS232C port (* section 2.5.1.6).

Weight

Type	Weight
FP10SH CPU	approx. 350 g/12.346 oz.
Expansion memory unit	approx. 30 g/1.058 oz.
IC memory card board	approx. 60 g/2.116 oz.
ROM operation board	approx. 35 g/1.235 oz.



2.5.1.1 Status Indicator LEDs

These LEDs display the current mode of operation or the occurrence of error.

LED	Description
RUN (green)	This lights in the RUN mode, to indicate that the program is being executed. It flashes during forced input/output.
PROG. (green)	This lights in the PROG. mode. Operation stops while this LED is lighted. It flashes when waiting for connection of a distributed slave station. If the memory is initialized, the brightness dims, indicating that initialization is being executed.
TEST (green)	This lights in the test mode.
BREAK (green)	This lights in the operation halts at a break during a test run or halts during the step operation mode for the test run.
ERROR (red)	This lights if an error is detected during the self–diagnostic function.
BATT. (red)	This lights when the voltage of the backup battery drops below a specific value.
ALARM (red)	This lights if a hardware error occurs, or if operation slows because of the program, and the watchdog timer is activated.

2.5.1.2 Initialize/Test Switch

This switch clears errors, initializes the memory, and sets the test operation mode. The setting of mode selector is relevant when initializing the CPU memory.

Switch position	Operation mode
INITIALIZE (upward)	**In the PROG. mode:** The contents of the operation memory are initialized. However, the system register (including the I/O map) and the program are not initialized. If a self−diagnostic error code of 42 or lower is occured, the special internal relays R9000 to R9008 and the special data register DT90000 are not cleared. **In the RUN mode:** Operation errors, remote I/O system errors, and battery errors are cleared.
(center)	The switch should normally be left in this position.
TEST (downward)	Setting this switch to the downward position in the PROG. mode, accesses the test mode. Switching to the RUN mode in this state, initiates test operation. To return from the test mode to the normal operation, return this switch to the center position in the PROG. mode.

☞ **Note**

With FP10SH CPU, by turning ON the Initialize/test switch while in the PROG. mode, you can specify the type of operation memory to be cleared with system register 4.

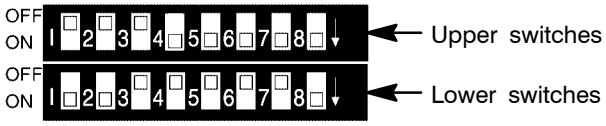
2.5.1.3 Mode Selector

Use the mode selector to start and stop the operation of the FP10SH CPU. For test operations, set the initialize/test switch to TEST position.

Selector position	Operation mode
RUN (upward)	This sets the RUN mode. The program is executed, and operation begins.
REMOTE (center)	This enables operation to be started and stopped from a programming tool. At the stage where the selector is changed, when switching from the PROG. to the REMOTE mode, the system remains in the PROG. mode, and when switching from the RUN to the REMOTE mode, it remains in the RUN mode.
PROG. (downward)	This sets the PROG. mode. In this mode, programming can be done using tools, the test mode can be accessed, and the operation memory can be initialized using the Initialize/tset switch.

2.5.1.4 Operation Condition Switches

Each switch has the function shown below assigned to it.



Upper switches

- Switches 1 through 8: Communication format settings for the COM port.

The settings written with bold characters are the default settings.

Functions			Settings							
			SW1	SW2	SW3	SW4	SW5	SW6	SW7	SW8
COM port settings	MODEM control (* Note 1)	Disabled	**OFF**							
		Enabled	ON							
	Header (* Note 2, 3)	STX (H02) invalid		**OFF**						
		STX (H02) valid		ON						
	Terminator (* Note 2)	None			OFF	OFF				
		CR (H0D) + LF (H0A)			ON	OFF				
		CR (H0D)			**OFF**	**ON**				
		ETX (H03)			ON	ON				
	Stop bit	2 bits					OFF			
		1 bit					**ON**			
	Parity check	Invalid						OFF	OFF	
		Even parity						ON	OFF	
		Odd parity						**ON**	**ON**	
	Character length	7 bits								OFF
		8 bits								**ON**

☞ **Notes**

- **(*1): MODEMs available for FP10SH CPU are Hays AT command compatible types for public line use.**
- **(*2): These functions are used for COM port's serial data communication with a field device. In order to use this, set the system register 412 to K2 (serial data commu nication mode) and control the communications using the F144 (TRNS)/P144 (PTRNS) instructions.**
- **(*3): Header is used to express the start of the communication frame. If header setting in the valid mode, CPU handle a series of data from STX header to terminator as a frame.**

Lower switches

- Switches 1 through 3: Transmission speed (baud rate) and communication format settings for the programming tool (Tool port).
- Switch 4: Set this switch to ON to disable writing to the program memory.
- Switch 5: Use this switch to set whether to use the internal RAM or optional memory as the program memory.
  When selecting optional memory after installing an IC memory card, the program file named AUTOEXEC in the IC memory card is automatically loaded into the internal RAM.
- Switches 6 through 8: Transmission speed (baud rate) settings for the COM port

The settings written with bold characters are the default settings.

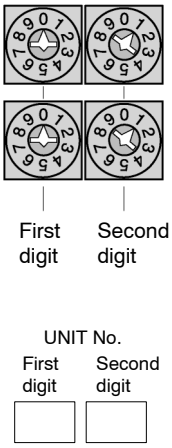
Functions			Settings							
			SW1	SW2	SW3	SW4	SW5	SW6	SW7	SW8
TOOL port settings	Transmission speed (baud rate)	19,200 bps (*Note 2)	OFF							
		9,600 bps	**ON**							
	Data length	7 bits		OFF						
		8 bits		**ON**						
	MODEM control (* Note 1)	Disabled			**OFF**					
		Enabled			ON					
Memory settings	Program memory protection	Write enabled				**OFF**				
		Write protected				ON				
	Program memory selection	CPU internal RAM					**OFF**			
		Using optional memory					ON			
COM port settings	Transmission speed (baud rate)	115,200 bps						OFF	OFF	OFF
		57,600 bps						ON	OFF	OFF
		38,400 bps						OFF	ON	OFF
		19,200 bps						ON	ON	OFF
		9,600 bps						**OFF**	**OFF**	**ON**
		4,800 bps						ON	OFF	ON
		2,400 bps						OFF	ON	ON
		1,200 bps						ON	ON	ON

☞ Notes

- **(*1): MODEMs available for FP10SH CPU are Hays AT command compatible types for public line use.**
- **(*2): Can be changed with the settings in system register 414.**

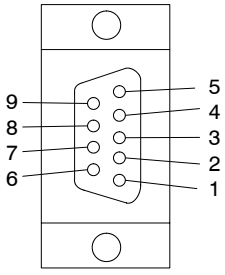
2.5.1.5 Station Number Setting Switches

Set the station number for the unit when using the computer link functions with the tool port and COM port of the CPU.
Be sure to set a station number in the range of 01 to 32.



2.5.1.6 COM Port (RS232C)

Pin alignment



Pin number	Signal name		Signal direction FP10SH–Field device
1	Frame ground	FG	
2	Send data	SD	→
3	Received data	RD	←
4	Request to send	RS	→
5	Clear to send	CS	←
6	Not used	–	
7	Signal ground terminal	SG	
8	Not used	–	
9	Equipment ready (always ON)	ER	→

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Communication specifications

The transmission speed and communication format are decided by the operation condition switches on the CPU (* section 2.5.1.4). The table below indicates the default settings.

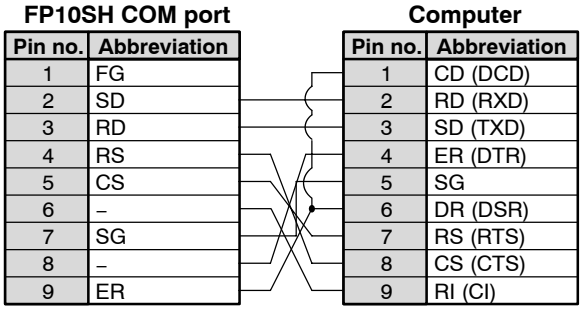
Item	Description
Transmission speed (baud rate)	9,600 bps
Character bit	8 bits
Parity check	Odd parity
Start bit	1 bit
Stop bit	1 bit
Header	STX invalid
Terminator	CR

In the computer link, header and terminator are decided by the MEWTOCOL-COM format.

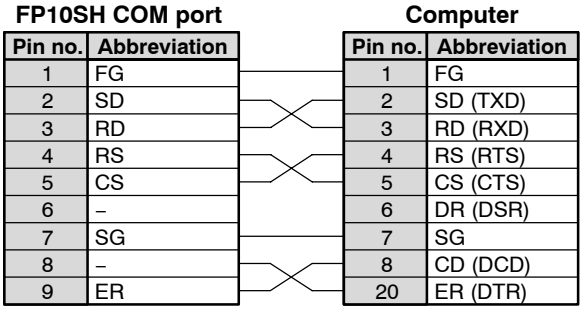
These settings are used for serial data communication with a field device. In order to use this, set the system register 412 to K2 (serial data communication mode) and control the communication with the **F144 (TRNS)**/**P144 (PTRNS)** instructions.
The serial data communication instructions **F144 (TRNS)**/**P144 (PTRNS)** cannot be executed unless pin number 5 (CS) of COM port (RS232C) is turned ON.

Connection cable examples

Example 1: Connected to a computer (9-pin)



Example 2: Connected to a computer (25-pin)



Example 3: Connected to a I.O.P. D series (9-pin)

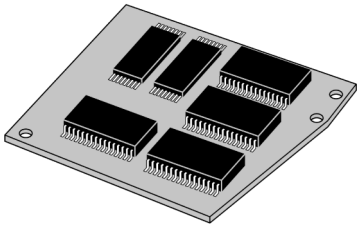
FP10SH COM port

Pin no.	Abbreviation
1	FG
2	SD
3	RD
4	RS
5	CS
6	–
7	SG
8	–
9	ER

I.O.P. D series

Pin no.	Abbreviation
1	–
2	SD
3	RD
4	RS
5	CS
6	–
7	SG
8	–
9	–

2.5.2 Expansion Memory Unit



The expansion memory unit is installed in the FP10SH CPU.
The expansion memory unit enables FP10SH to expand program memory up to 60 k or 120 k steps using two following types:

Type	Order number	Weight
30 k steps type	AFP6204	approx. 30 g/1.058 oz.
90 k steps type	AFP6205	

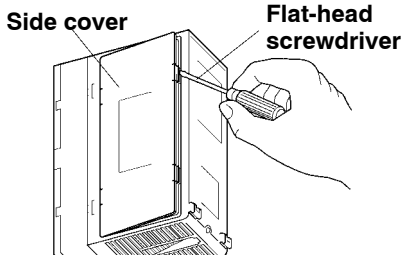
☞ **Note**

When installing and removing an expansion memory unit, the contents of built–in RAM of CPU may be destroyed. Be sure to make backup of program stored in the built–in RAM of CPU before installing and removing an expansion memory unit. And, if you need, re-transfer the program to the CPU using NPST–GR software, after installation.

Installing the expansion memory unit

Procedure:

1. **Remove the side cover of the FP10SH CPU with a flat-head screwdriver.**



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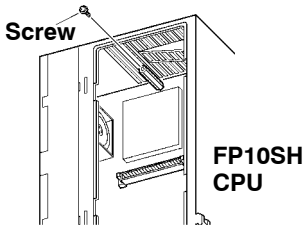
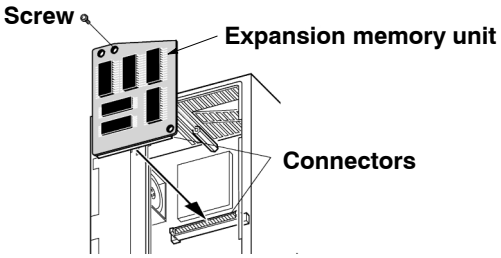
2. Loosen the screw in the FP10SH CPU.



3. Properly connect the expansion memory unit to the CPU's connector. Then, secure the fixing screw.



☞ **Notes**

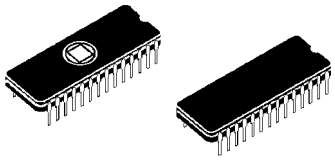
- **Be sure to turn OFF the power before installing and removing the expansion memory unit.**
- **Never touch the ICs or connectors when handling the expansion memory unit.**

2.5.3 ROM Operation Board

The FP10SH can be operated using only the installed built–in RAM, but use of commercially available EPROM/FROM is also possible if necessary.

The ROM operation board is necessary for ROM operation.

Memory (EPROM) and Master Memory (FROM)



Attach to the ROM operation board for operation.
The memory (EPROM) should be used for program storage and ROM operation, and the master memory (FROM) should be used for copying and transferring programs.

CPU Ver. 2 or later is required to use the memory.

Type of FP10SH optional memories

Type	Memory (EPROM)	Master memory (FROM)
Using I.C.	M27C2001–150F1 or equivalent	SST–29EE020–150–4C–PH or equivalent
Order number	AFP5209	AFP5208
Writing method	Commercially available ROM programmer	You can write program to FROM installing it on the CPU.
Use	Suitable for program storage or ROM operation	Suitable for copying and transmitting the master program

☞ **Note**

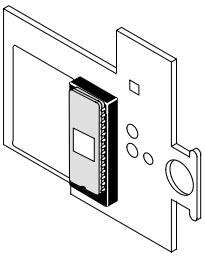
The I/O comments are written to the internal memory of the ROM operation board.

Comments written to ROM

The program, system register, and initial settings (memory contents and user selections for DT and other settings) are written to the memory (EPROM) or master memory (FROM). Therefore, for ROM operation, be aware that the program contents and data register (operation data) contents are simultaneously rewritten.

The comments (line comments, comment statements, and I/O comments) are stored in the internal memory of the ROM operation board.

ROM Operation Board

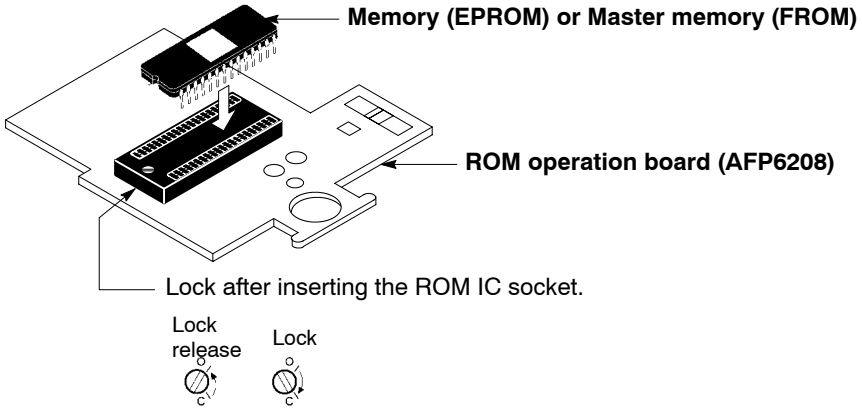


The ROM operation board is for installing the optional memory (ROM). Install the memory (EPROM) and master memory (FROM) onto the board and insert the board into the CPU.

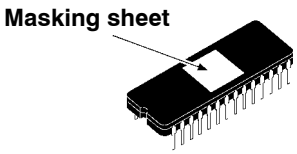
Item	Description
Order number	AFP6208
Weight	approx. 35 g/1.235 oz.

☞ Notes

- **When installing the optional memory (EPROM or FROM) to the ROM operation board, carefully adjust the pitch of the memory IC leads to the width of the leads for the IC socket and securely insert the ICs in the correct orientation (with the grooves facing in the correct direction). After inserting the optional memory, securely lock it into place.**



- **When removing the ROM from the IC socket, first unlock it from the socket.**
- **Always attach a masking sheet to cover the window of the memory (EPROM). If the masking sheet is not attached, flashes and other light sources may cause misoperation.**

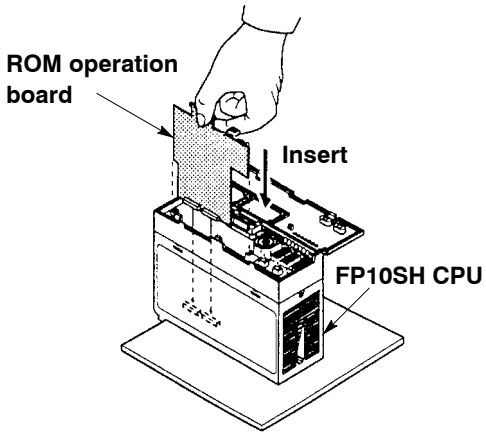


Installing the ROM operation board

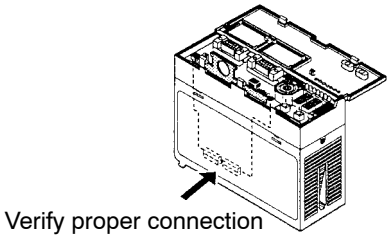
When installing the ROM operation board, first remove the FP10SH CPU from its backplane.

Procedure:

1. **Place the CPU down flat on a surface and insert the ROM operation board into the CPU along the guides provided. At this time, make sure that the hook on the bottom of the CPU used for attaching the unit to the backplane is located off the table you are working on.**



2. **Align the ROM operation board with its connector on the bottom of the CPU. To make sure that the board is properly attached, confirm it visually by looking through the holes on the side of the CPU. If the board is inserted while not aligned with the connector, the pins of the board may become bent.**



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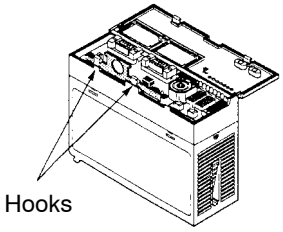
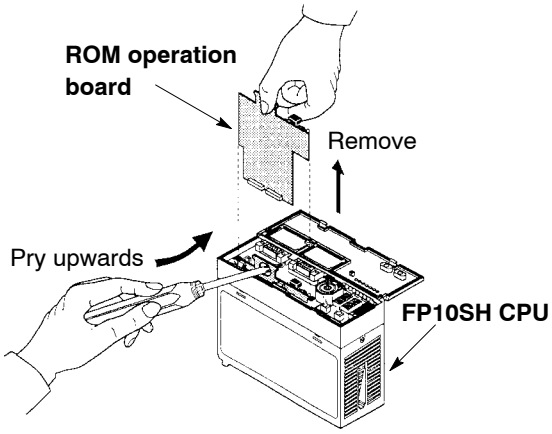
3. Firmly press on the ROM operation board from above and insert it into its connector. Firmly insert the board until its upper frame is caught on the hooks of the CPU (continue pushing until a catching sound is heard).



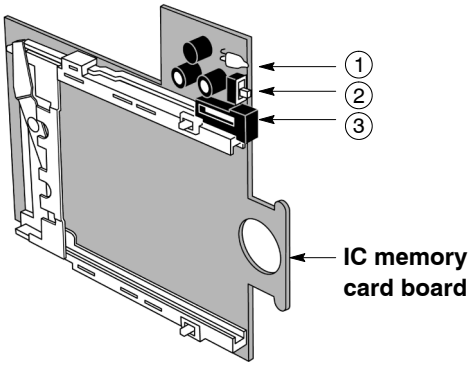
4. To remove the board, unhook the hook by hand, insert a screwdriver into the hole provided and pry the board upwards.



2.5.4 IC Memory Card Board

In order to install the IC memory card in the FP10SH CPU, the IC memory card board is required.

Item	Description
Order number	AFP6209A
Weight	approx. 60 g/2.116 oz.



① **IC memory card access LED**
Illuminates when data is being read from or written to the IC memory card.
When lit ------ Accessing
When not lit --- Not accessing

② **IC memory card access enable switch**
Use to enable reading from and writing to the IC memory card.

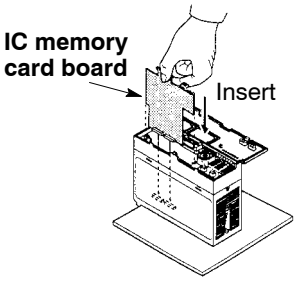
ON ---- Read and write enable
OFF --- Read and write disable

③ **IC memory card eject button**
Use to remove the IC memory card.

Installing the IC memory card board
When installing the IC memory card board, first remove the FP10SH CPU from its backplane.

Procedure:

1. **Place the CPU down flat on a surface and insert the IC memory card board into the CPU along the guides provided.**
   At this time, make sure that the hook on the bottom of the CPU used for attaching the unit to the backplane is located off the table you are working on.



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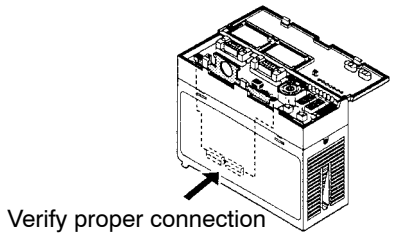
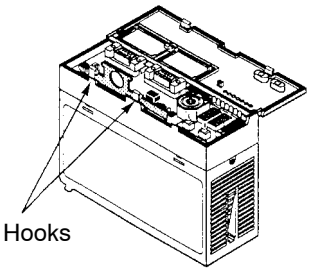
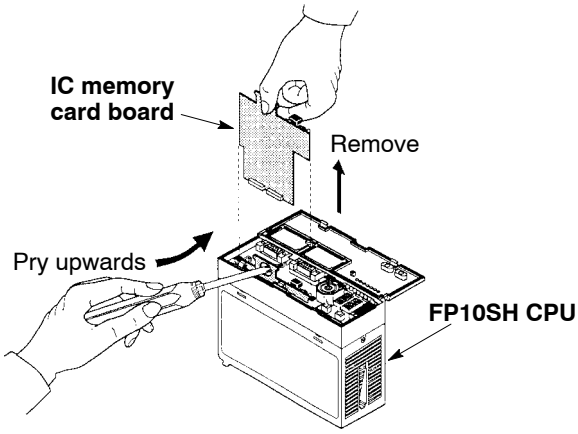
2. **Align the IC memory card board with its connector on the bottom of the CPU. To make sure that the board is properly attached, confirm it visually by looking through the holes on the side of the CPU. If the board is inserted while not aligned with the connector, the pins of the board may become bent.**



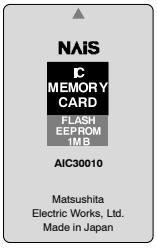
3. **Firmly press on the IC memory card board from above and insert it into its connector. Firmly insert the board until its upper frame is caught on the hooks of the CPU (continue pushing until a catching sound is heard).**



4. **To remove the board, unhook the hook by hand, insert a screwdriver into the hole provided and pry the board upwards.**



2.5.5 IC Memory Card



The IC memory card can be used for program storage or copies or as expansion memory for reading and writing data from the program.

The IC memory card can be divided into a MS–DOS format area for storing various programs and an expansion memory area for data storage.

Example: If a 1 MB card is formatted for 512 KB, then 512 KB can be used for the MS–DOS format area and the remaining 512 KB can be used for the expansion memory area.

The card can be used exclusively for program storage or exclusively for data memory by using the full memory area for the MS–DOS format area or the expansion memory area.

When the FLASH-EEPROM area is designated as an expansion memory area, then the card becomes read only.

Type	Memory capacity	Order number	Usage		Recommended usage
			Program storage	Expansion memory area	
S-RAM type	1 MB	AIC31000	Write using the NPST-GR **"IC CARD PROGRAM MANAGER"** menu.	Write using the **F13 (ICWT)**/ **P13 (PICWT)** instruction. Read using **F12 (ICRD)**/ **P12 (PICRD)** instruction.	Because data can be read or written from the program, this type is ideal for expansion data memory.
FLASH-EEPROM type	1 MB	AIC30010	Write using the NPST-GR **"IC CARD PROGRAM MANAGER"** menu.	Becomes read-only memory. Read using **F12 (ICRD)**/ **P12 (PICRD)** instruction.	Because backup battery is not required, this type is ideal for program storage.

☞ next page

☞ **Notes**

- **Both the S-RAM type and FLASH-ROM type can also be divided into MS–DOS format area and expansion memory area.**
- **When using the IC memory card for program memory, there are three methods for reading the program:**
  - **Automatic read at power ON.**
  - **Read using the NPST-GR software "IC CARD PROGRAM MANAGER" menu.**
  - **Read using F14 (PGRD)/P14 (PPGRD) instruction.**

Handling the IC memory card

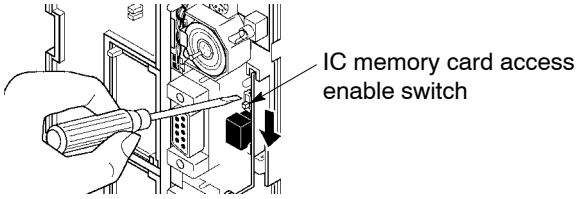
- **Avoid subjecting the card to high temperature, high humidity, and direct sunlight.**
- **Do not bend or subject to strong impact.**
- **Do not touch or allow foreign materials to enter the connector part.**
- **Never throw the card into a fire.**

Inserting and removing the IC memory card

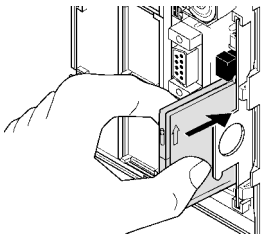
The IC memory card can be inserted or removed even when the FP10SH power is ON. To insert or remove the card when the power is ON, be sure to follow the following procedure.

Insertion procedure:

1. **Set the IC memory card access enable switch to OFF position.**



2. **Insert the IC memory card into the slot.**



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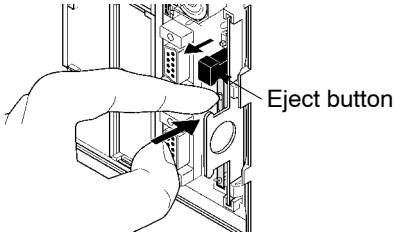
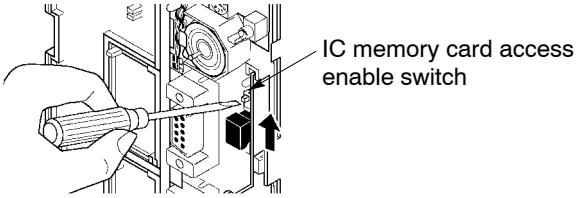
3. **Continue pushing the IC memory card until the eject button pops out.**



4. **Set the IC memory card access enable switch to ON position.**

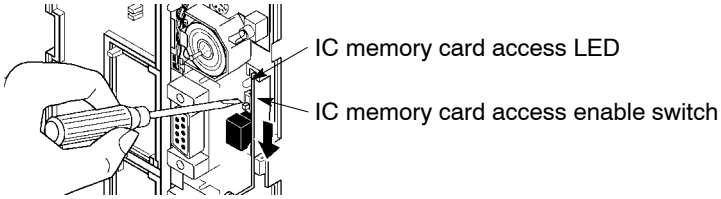


☞ **Notes**

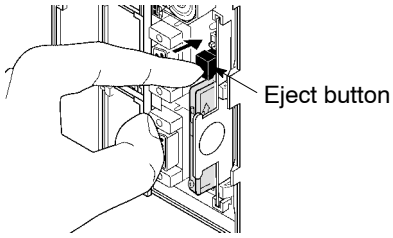
- **Do not try to insert the IC memory card while the IC memory card access enable switch is ON. It could lead to damage of the memory contents or a malfunction of the CPU.**
- **Do not use excessive force on the IC memory card or slot.**

Removal procedure:

1. **Set the IC memory card access enable switch to OFF position. Verify that the IC memory card access LED is OFF.**



2. **Push the eject button until the IC memory card becomes free.**



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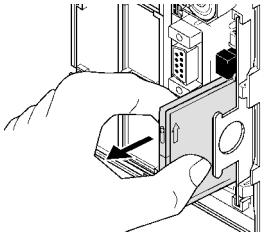
3. **Pull out the IC memory card.**



☞ **Notes**

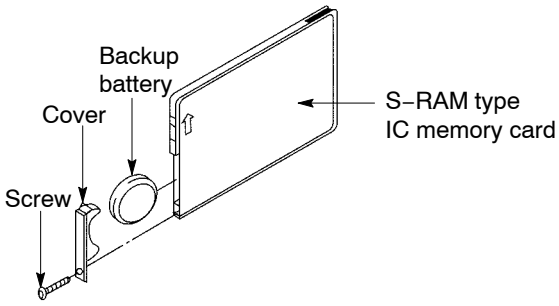
- **Do not try to remove the IC memory card while the IC memory card access enable switch is ON. It could lead to damage of the memory contents or a malfunction of the CPU.**
- **Do not use excessive force on the IC memory card or slot.**

Battery for S-RAM type IC memory card

The S-RAM type IC memory card is backed up by a battery. Be sure to set the battery in the card before insertion into the CPU.

Procedure:

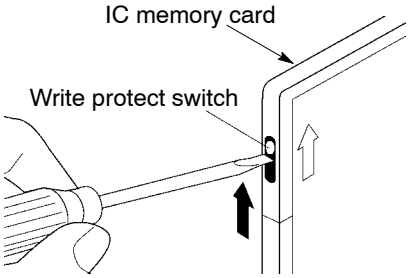
1. **Use the screwdriver supplied with the IC memory card to remove the screw on the card side.**
2. **Set the accessory backup battery. Make sure the direction of the battery is correct.**
3. **Attach the cover and screw in place.**



Refer to section 8.1.2 for an explanation of the backup battery life and replacement method.

IC memory card write protection

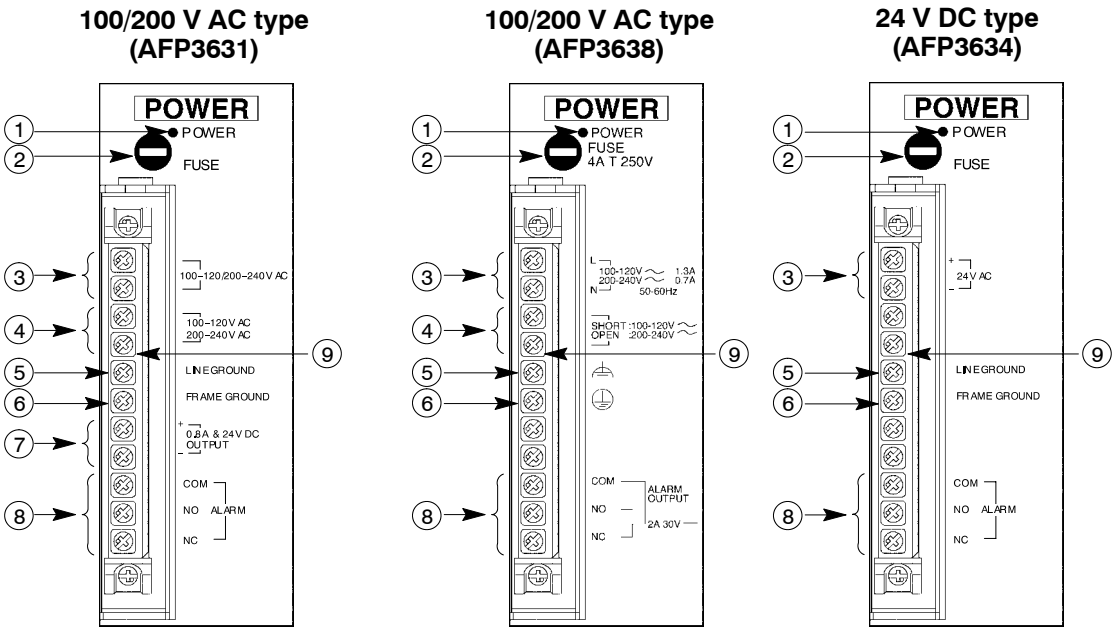
There is a write protect switch on the IC memory card. To prohibit writes to the IC memory card, set this switch to WP position.



☞ **Note**

To write the program or data to the IC memory card, set the write protect switch to protect OFF position.

2.6 Power Supply Units



Parts Terminology and Functions

① **POWER LED**
Turns ON when power is applied to the unit.

② **Power supply fuse holder**

③ **Power supply terminal**
AC type: This terminal is the terminal for 100 to 240 V AC.
DC type: This terminal is the terminal for 24 V DC.

④ **Voltage selecting terminals (for AFP3631 and AFP3638)**
When the supply voltage is in the 100 to 120 V AC range, short the terminals with the supplied jumper.
Check that the terminals are open when the supply voltage is in the 200 to 240 V AC range.
The terminals are open when shipped from the factory.

⑤ **Line ground terminal**
is the terminal for the built–in line filter. To minimize effects from noise and prevent electrical shocks, ground this terminal together with the frame ground terminal.

⑥ **Frame ground terminal**
is connected to a metal portion of the backplane.
To prevent electrical shocks, connect this terminal to ground.

☞ next page

⑦ **Service power terminal (24 V DC) (for AFP3631 only)**
Used for the DC power supply (24 V DC) for the I/O units. The capacity will differ depending on the type of power supply unit. Do not connect this service power terminal in parallel with the power supply for other commercially available power supply devices.

⑧ **Alarm output terminal**
Contact output terminals of the relay which turns ON when the ALARM LED of the CPU turns ON. Normally closed contact (N.C.) and normally open contact (N.O.) are available.
However, this relay operates only when the power supply unit is installed in the master backplane.

⑨ **Terminal block**
is the terminal for power supply wiring. Uses M3.5 crimp terminals
(* section 4.2.1).

2.6.1 Power Supply Specifications

Item		AC type		DC type
Order number		**AFP3631**	**AFP3638**	**AFP3634**
Rated input voltage		100 to 120 V AC or 200 to 240 V AC (voltage selectable)		24 V DC
Operating voltage range		85 to 132 V AC or 170 to 264 V AC		16.8 to 28.8 V DC
Rated frequency		47 to 63 Hz		——
Surge current		20 A or less		
Current consumption		0.9 A or less (at 100 V AC) 0.5 A or less (at 200 V AC)	1.3 A or less (at 100 V AC) 0.7 A or less (at 200 V AC)	1.0 A or less (at 24 V DC)
Rated output current (* Note)	**5 V DC**	2.4 A	9 A (at ambient temperature 45 °C/ 113 °F or less) 7A (at ambient temperature 55 °C/ 131 °F or less)	2.4 A
	24 V DC	0.8 A	——	——
Alarm contact rated control capacity		2 A 250 V AC, 2 A 30 V DC		2 A 30 V DC
Weight		approx. 600 g/21.164 oz.		approx. 500 g/ 17.637 oz.

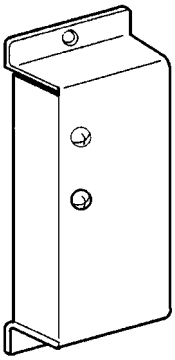
☞ **Note**

The rated output current for 5 V DC indicates the current from the power supply unit that can be supplied through the backplane to each unit. The rated output current for 24 V DC indicates the current from the service power terminal that can be supplied to the I/O units and other units.

CAUTION (AFP3638 only)

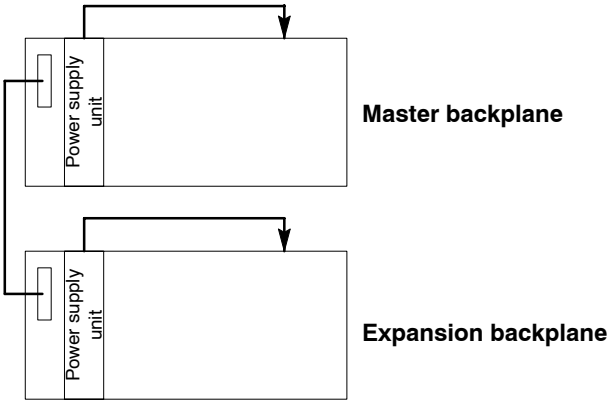
- **When expanding units, it is necessary to use the same type of power supply units between basic backplane and expansion backplane.**
- **When using the D/A converter unit, up to 6 units can be expanded on one backplane.**
  (The consumption current of the power supply unit is temporarily rise when the power is supplied. The system does not work for excessive current protection if the excessive current flow.)

2.7 Power Supply Dummy Unit

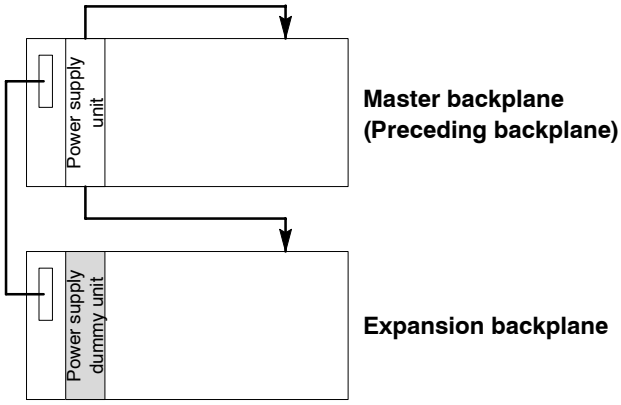


If the internal current consumption used for the expansion backplanes is small, this power supply dummy unit can be installed in place of the unnecessary power supply unit on the expansion backplane.

<Normal setup installation>
The power supply used on each backplane is provided by a power supply unit installed on that backplane.



<Setup with a power supply dummy unit>
The power supply for the expansion backplane with the power supply dummy unit installed is provided by the power supply unit on the preceding backplane.



2.7.1 Conditions for Using a Power Supply Dummy Unit

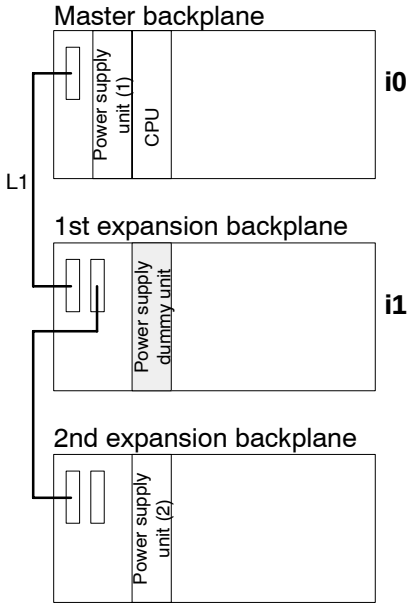
A power supply dummy unit can be installed on an expansion backplane if the following conditions are satisfied:

- The length of the expansion cable which connects the backplane installed with a power supply dummy unit and the preceding backplane must be shorter than 3 m/9.8 ft..
- The total value (i1) of the internal current consumption at 5 V DC of the backplane installed with the power supply dummy unit is less than 1.0 A.
- The sum of the total value (i1) of the internal current consumption at 5 V DC of the backplane installed with the power supply dummy unit and total value (i0) of the internal current consumption at 5 V DC of the preceding backplane is less than the rated current value of the power supply unit.

☞ **Note**

You cannot use two power supply dummy units in series.

Example 1:
When the power supply dummy unit is installed on the 1st expansion backplane



Conditions

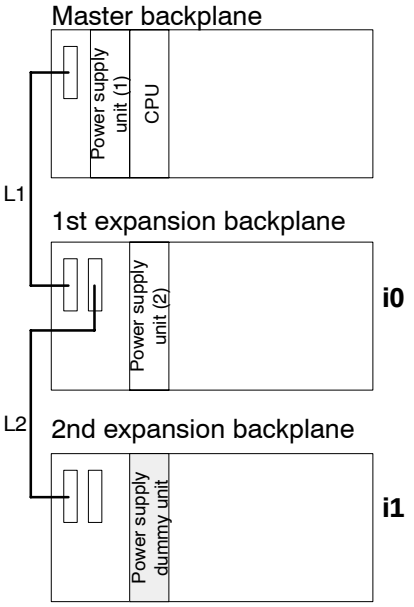
- **i0 + i1 ≦ Rated current value of power supply unit (1)**
- **i1 ≦ 1 A**
- **L1 ≦ 3 m/9.8 ft.**

i0: Total value of internal current consumption at 5 V DC of the master backplane with the power supply unit (1).

i1: Total value of internal current consumption at 5 V DC of the 1st expansion backplane with the power supply dummy unit.

L1: Length of expansion cable between the master backplane and the 1st expansion backplane.

Example 2:
When the power supply dummy unit is installed on the 2nd expansion backplane



Conditions

- **i0 + i1 ≦ Rated current value of power supply unit (2)**
- **i1 ≦ 1 A**
- **L2 ≦ 3 m/9.8 ft.**

i0: Total value of internal current consumption at 5 V DC of the 1st expansion backplane with the power supply unit (2).

i1: Total value of internal current consumption at 5 V DC of the 2nd expansion backplane with the power supply dummy unit.

L2: Length of the expansion cable between the 1st expansion backplane and the 2nd expansion backplane .

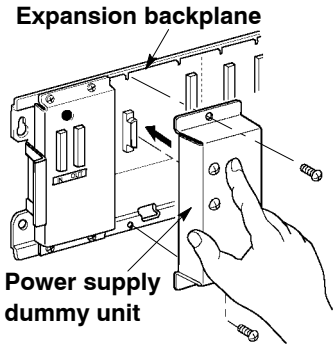
☞ **Note**

Refor to section 1.3.3, for detalis about the current consumption of each unit.

2.7.2 Installing the Power Supply Dummy Unit

Procedure:

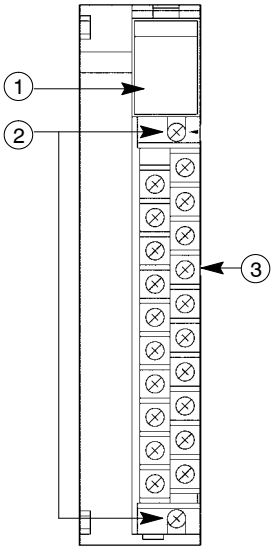
1. **Align the connector on the rear of the power supply dummy unit with the power supply connector on the expansion backplane.**



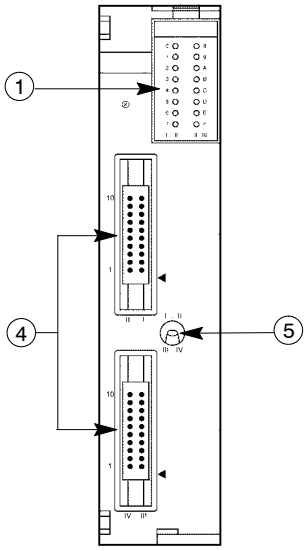
2. **Secure the power supply dummy unit to the expansion backplane with the installation screws provided.**

2.8 Common Specifications of Input, Output and I/O Mixed Units

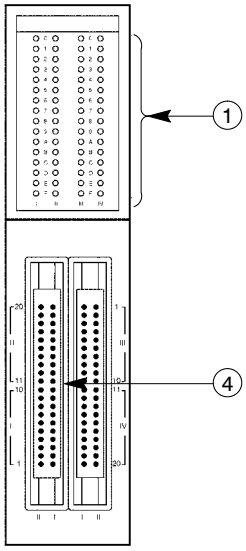
8–point/16–point



32–point



64–point



Parts Terminology and Functions

① **Input and output indicators**
Indicate the ON/OFF states of input and output.

② **Terminal fixing screws**
The terminal block can be removed by loosening the two screws.

③ **Terminal block**
Input, output and power supply wiring section for the 8-point and 16-point types. Uses M3.5 pressure connection terminals (* section 4.2.1).

④ **Connectors (32–points type: 20–pin × 2, 64–points type: 40–pin × 2)**
Input, output and power supply wiring section for the 32-point and 64-point types. You can use either discrete–wire connectors or flat cable connectors (* section 4.4).

⑤ **Selector for input and output indicators**
Selects the inputs and output that will be represented by the input and output indicators. When this selector is set to the up position, the input and output ON/OFF states for the first 16-point are indicated and when set to the down position, the states for the last 16-points are indicated.

2.8.1 Table of Input Unit Types

Type	Number of points	Connection method	Description	Order number
DC input type	**16-point**	terminal	12 to 24 V DC, sink/source input	AFP33023–F
	32-point	connector	12 to 24 V DC, sink/source input	AFP33024–F
			5 V DC, sink/source input	AFP33014–F
	64-point	connector	12 to 24 V DC, sink/source input	AFP33027–F
			5 V DC, sink/source input	AFP33017–F
			high-speed response type, 12 to 24 V DC, sink/source input	AFP33028–F
			high-speed response type, 24 V DC, sink/source input	AFP33068–F
AC input type	**8-point**	terminal	100 to 120 V AC	AFP33041
			200 to 240 V AC	AFP33051
	16-point	terminal	100 to 120 V AC	AFP33043
			200 to 240 V AC	AFP33053

2.8.2 Table of Output Unit Types

Type	Number of points	Connection method	Description	Order number
Relay output type	**16-point**	terminal	without relay sockets, 2 A/point	AFP33103–F
			with relay sockets, 2 A/point	AFP33203–F
Transistor (NPN open collector) output type	**16-point**	terminal	5 to 24 V DC, 0.5 A	AFP33483–F
	32-point	connector	5 to 24 V DC, 0.1 A	AFP33484–F
	64-point		5 to 24 V DC, 0.1 A	AFP33487–F
Transistor (PNP open collector) output type	**16-point**	terminal	5 to 24 V DC, 0.1 A	AFP33583–F
	32-point	connector	5 to 24 V DC, 0.1 A	AFP33584–F
	64-point		5 to 24 V DC, 0.1 A	AFP33587–F
Triac output type	**16-point**	terminal	100 to 240 V AC, 0.5 A/point	AFP33703

☞ **Note**

The maximum load current for the transistor output type output unit will differ depending on the voltage used.
Refer to the specifications pages for each unit.

2.8.3 Table of I/O Mixed Unit Types

Type	Number of points	Connection method	Description	Order number
DC input/ Relay output type	**16-point (I: 8 O: 8)**	terminal	Input: 12 to 24 V DC, sink/source input Output: 2 A, with relay sockets	AFP33223−F
DC input/ Transistor (NPN open collector) output type	**64-point (I: 32 O: 32)**	connector	Input: 12 to 24 V DC, sink/source input Output: 5 to 24 V DC, 0.1 A	AFP33428−F
DC input/ Transistor (PNP open collector) output type	**64-point (I: 32 O: 32)**	connector	Input: 12 to 24 V DC, sink/source input Output: 5 to 24 V DC, 0.1 A	AFP33528−F

2.9 Input Units Specifications

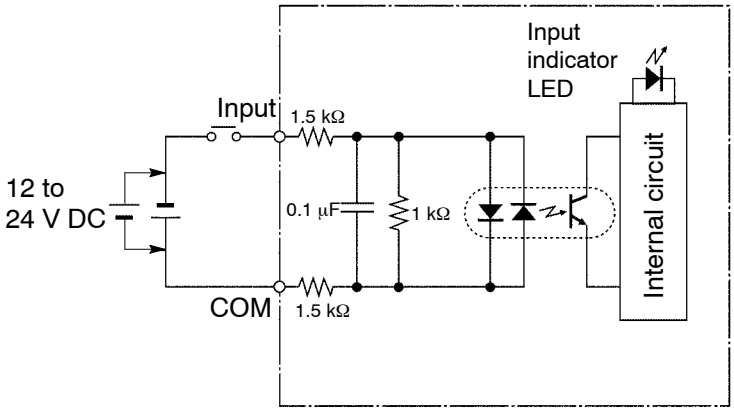
2.9.1 16-point Type DC Input Unit

2.9.1.1 Specifications

Item		Description
Order number		AFP33023−F
Rated input voltage		12 to 24 V DC
Rated input current		approx. 8 mA (at 24 V DC)
Input impedance		approx. 3 k Ω
Input voltage range		10.2 to 26.4 V DC (max. input current: 10 mA or less)
Min. ON voltage/ Min. ON current		9.6 V/4 mA
Max. OFF voltage/ Max. OFF current		2.5 V/1 mA
Response time	**OFF → ON**	1.5 ms or less
	ON → OFF	2.0 ms or less
Internal current consumption (at 5 V DC)		60 mA or less
Input points per common		8 points/common Either the positive or negative of the input power supply can be connected to COM (common) terminal.
Connection method		terminal block (M 3.5 screw)
Weight		approx. 300 g/10.582 oz

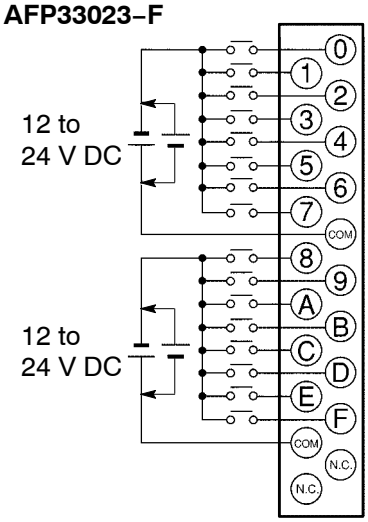
2.9.1.2 Internal Circuit Diagram

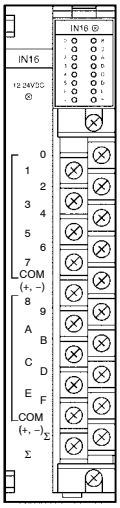
AFP33023−F



2.9.1.3 Pin Layout of Terminal Block

AFP33023−F





☞ **Note**

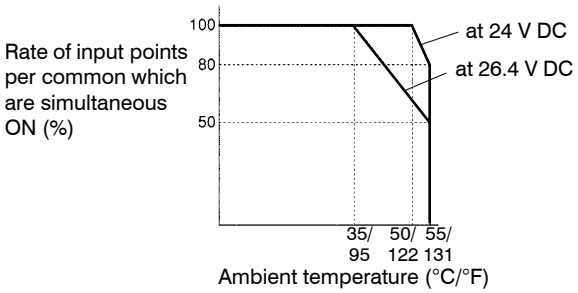
For more information regarding the applicable pressure connection (crimp) terminals and wiring, refer to section 4.5.

2.9.2 32-point Type DC Input Units

2.9.2.1 Specifications

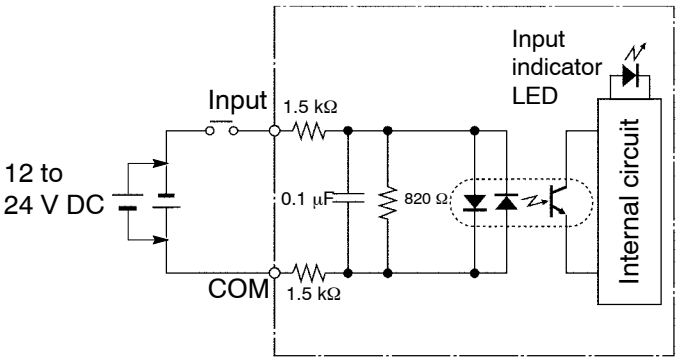
Item		Description	
Order number		AFP33024−F	AFP33014−F
Rated input voltage		12 to 24 V DC	5 V DC
Rated input current		approx. 8 mA (at 24 V DC)	approx. 4.2 mA (at 5 V DC)
Input impedance		approx. 3 k Ω	approx. 1.2 k Ω
Input voltage range		10.2 to 26.4 V DC	4.25 to 5.5 V DC
Min. ON voltage/ Min. ON current		9.6 V/4 mA	3.5 V/3 mA
Max. OFF voltage/ Max. OFF current		2.5 V/1 mA	1.5 V/1 mA
Response time	**OFF → ON**	1.5 ms or less	
	ON → OFF	2.0 ms or less	
Internal current consumption (at 5 V DC)		120 mA or less	
Input points per common		16 points/common Either the positive or negative of the input power supply can be connected to COM (common) terminal.	
Connection method		two 20-pin connectors	
Weight		approx. 400 g/14.110 oz	

When an AFP33024−F is used, keep the rate of input points per common which are simultaneously ON within the following range as determined by the ambient temperature.

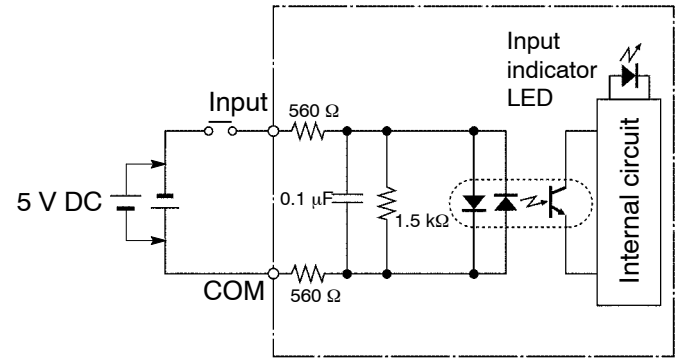


2.9.2.2 Internal Circuit Diagram

AFP33024–F

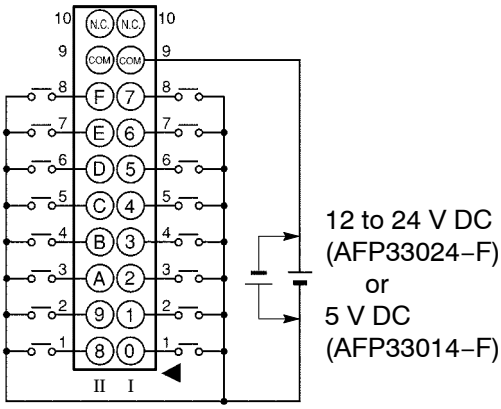


AFP33014–F

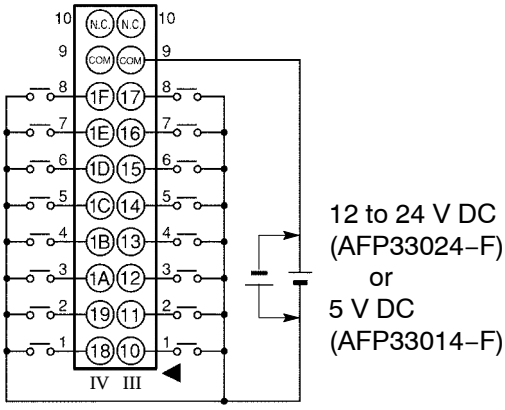


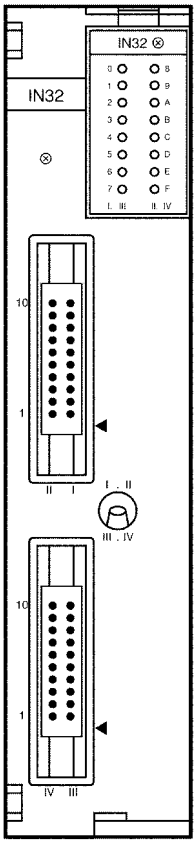
2.9.2.3 Pin Layout of Connector

Pin layout of first 16 points



Pin layout of last 16 points





☞ **Notes**

- **COM terminals for I and II are internally connected.**
- **COM terminals for III and IV are internally connected.**
- **For more information regarding the applicable connectors and terminals, refer to section 4.4.**

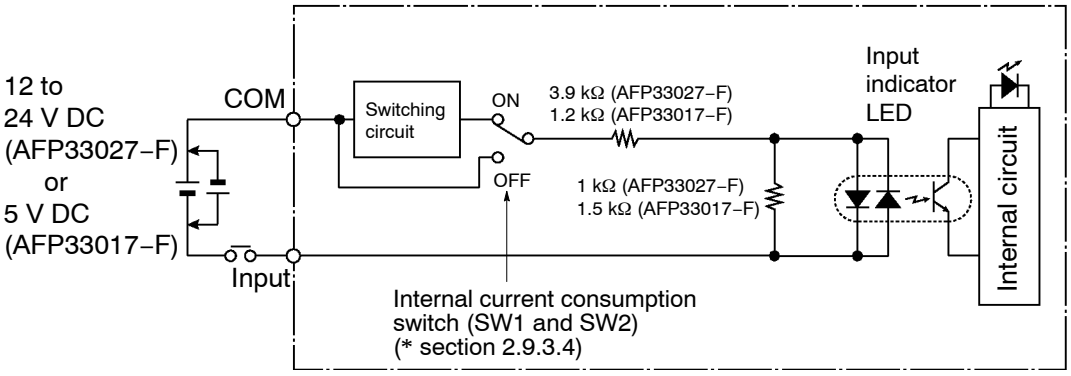
2.9.3 64-point Type DC Input Units

2.9.3.1 Specifications

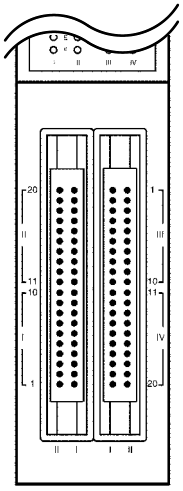
Item		Description	
Order number		AFP33027−F	AFP33017−F
Rated input voltage		12 to 24 V DC	5 V DC
Rated input current		approx. 6.2 mA (at 24 V DC)	approx. 4.2 mA (at 5 V DC)
Input impedance		approx. 3.9 k Ω	approx. 1.2 k Ω
Input voltage range		10.2 to 26.4 V DC	4.25 to 5.5 V DC
Min. ON voltage/ Min. ON current		9.6 V/3 mA	3.5 V/3 mA
Max. OFF voltage/ Max. OFF current		2.5 V/1 mA	1.5 V/1 mA
Response time	**OFF → ON**	1.5 ms or less	
	ON → OFF	2.0 ms or less	
Internal current consumption (at 5 V DC)		230 mA or less	
Input points per common		32 points/common Either the positive or negative of the input power supply can be connected to COM (common) terminal.	
Connection method		two 40-pin connectors	
Weight		approx. 400 g/14.110 oz	

2.9.3.2 Internal Circuit Diagram

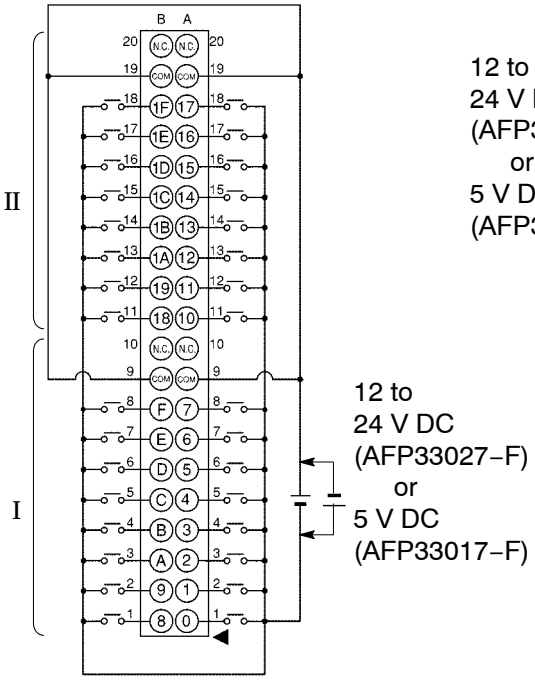
AFP33017−F/AFP33027−F



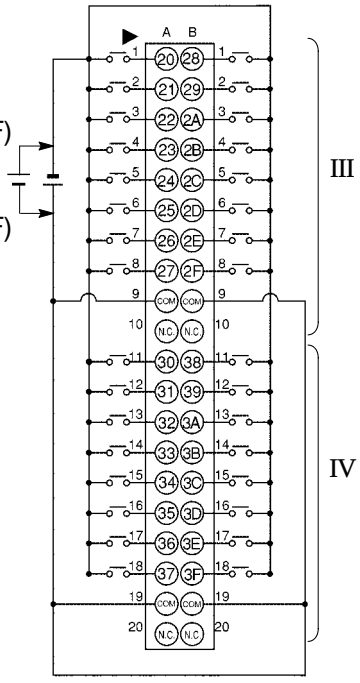
2.9.3.3 Pin Layout of Connector



Pin layout of first 32 points left side connector



Pin layout of last 32 points right side connector



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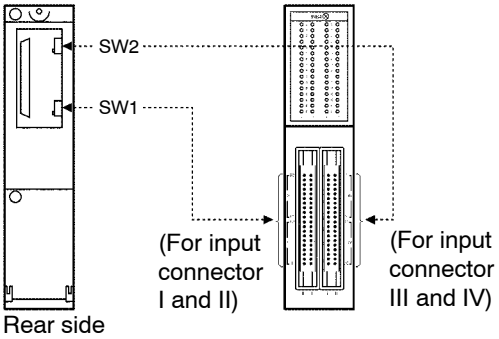
☞ **Notes**

- **COM terminals for I and II are internally connected.**
- **COM terminals for III and IV are internally connected.**
- **For more information regarding the applicable connectors and terminals, refer to section 4.4.**

2.9.3.4 Internal Current Consumption Switch

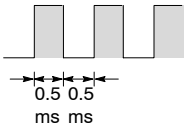
The 64-point type input unit has an internal switching circuit using non-contact relays to limit the current consumption of the internal circuit as shown in the internal circuit diagram (* section 2.9.3.2).

The internal circuit can be switched using the internal current consumption switches (SW1 and SW2) on the rear of the unit. The SW1 corresponds to the circuit for the input connector (I and II) on the left side of the unit, while the SW2 corresponds to the circuit for the input connector (III and IV) on the right side of the unit.



The operation of the circuit differs as follows according to whether the internal current consumption switch is ON or OFF.

– When this switch is ON
  The switching circuit is activated. A voltage with a pulse waveform is applied to the internal circuit of the 64–point type input unit.

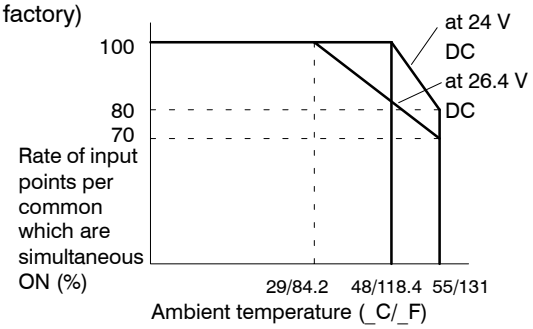


– When this switch is OFF
  The externally supplied voltage is applied as is to the internal circuit of the input unit. However, compared to when the this switch is ON, the internal current consumption is large so that, as shown in the graph (* section 2.9.3.5 on next page), the relative conditions become more severe.

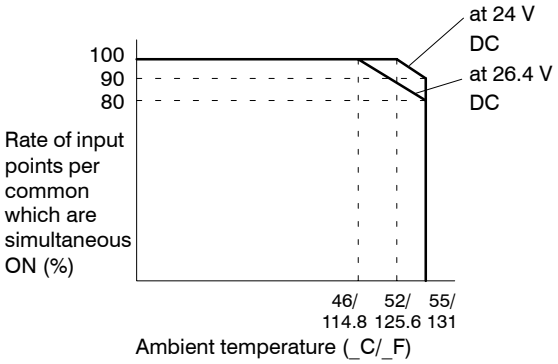
2.9.3.5 Limitations on Number of Simultaneous Input ON Points

Keep the number of input points per common which are simultaneously ON within the following range as determined by the temperature.

When internal current consumption switch SW1 and SW2 are both OFF
(settings at time of shipment from the factory)



When either internal current consumption switch SW1 or SW2 is ON



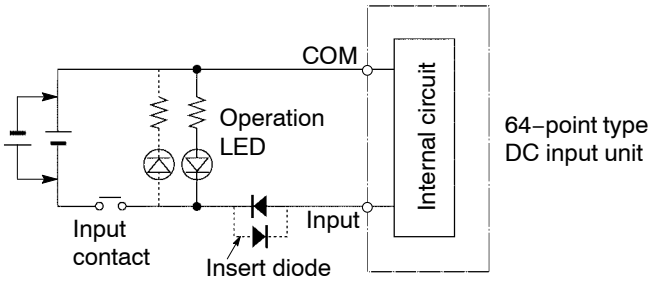
There is no limit when the internal current consumption switch SW1 and SW2 are both ON.

There is no limit when using 12 V DC.

2.9.3.6 Notes Regarding the Internal Current Consumption Switch Settings

When using two-wire type sensor or proximity sensors, be sure to turn OFF the internal current consumption switch corresponding to the circuit connected to the sensor.

When adding an operation verification LED in parallel with the input contact, or depending on the type of sensor used, there is a danger that the current will leak into another input circuit and cause erroneous operation. When this happens, either turn OFF the internal current consumption switch to the problem circuit or insert a diode into the input circuit (* section 4.3.1.6).



☞ **Note**

The dotted line represents reversal of input voltage polarity.

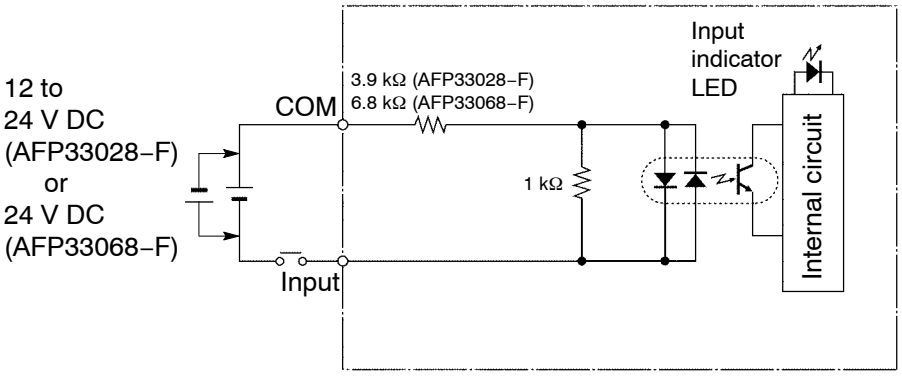
2.9.4 64-point/High−speed Response Type DC Input Units

2.9.4.1 Specifications

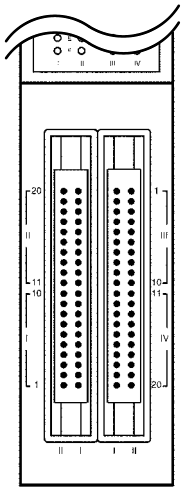
Item		Description	
Order number		AFP33028−F	AFP33068−F
Rated input voltage		12 to 24 V DC	24 V DC
Rated input current		approx. 6.2 mA (at 24 V DC)	approx. 3.5 mA (at 24 V DC)
Input impedance		approx. 3.9 k Ω	approx. 6.8 k Ω
Input voltage range		10.2 to 26.4 V DC	20.4 to 26.4 V DC
Min. ON voltage/ Min. ON current		9.6 V/3 mA	17.6 V/3 mA
Max. OFF voltage/ Max. OFF current		2.5 V/1 mA	5.0 V/1 mA
Response time	**OFF → ON**	0.1 ms or less	
	ON → OFF	0.3 ms or less	
Internal current consumption (at 5 V DC)		230 mA or less	
Input points per common		32 points/common Either the positive or negative of the input power supply can be connected to COM (common) terminal.	
Connection method		two 40-pin connectors	
Weight		approx. 400 g/14.110 oz	

2.9.4.2 Internal Circuit Diagram

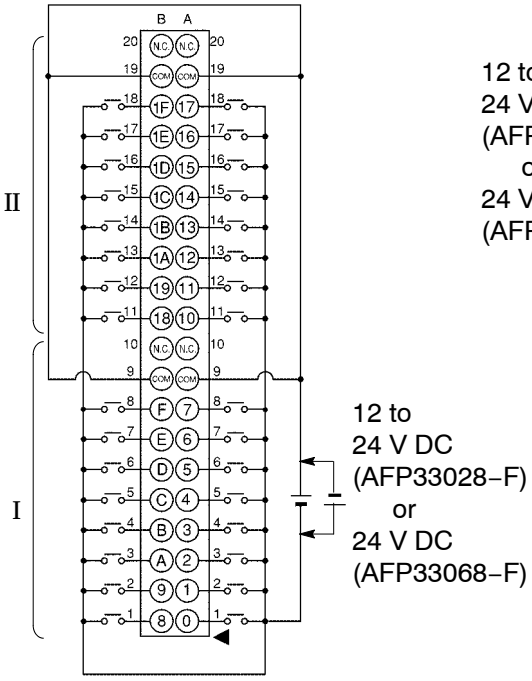
AFP33028−F/AFP33068−F



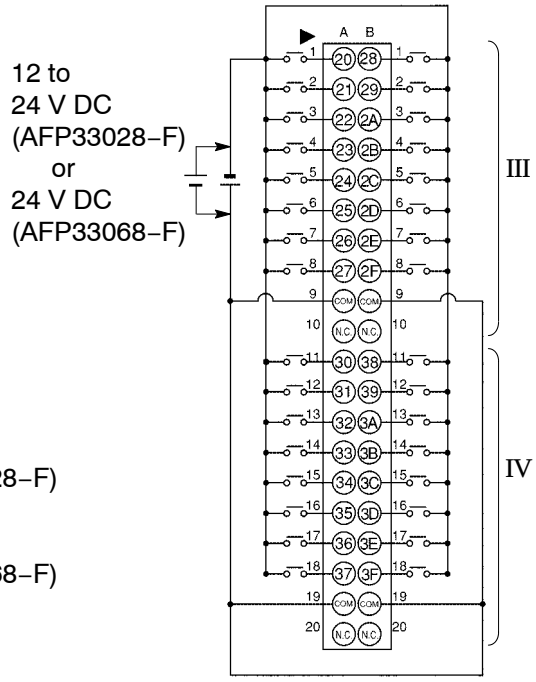
2.9.4.3 Pin Layout of Connector



Pin layout of first 32 points left side connector



Pin layout of last 32 points right side connector



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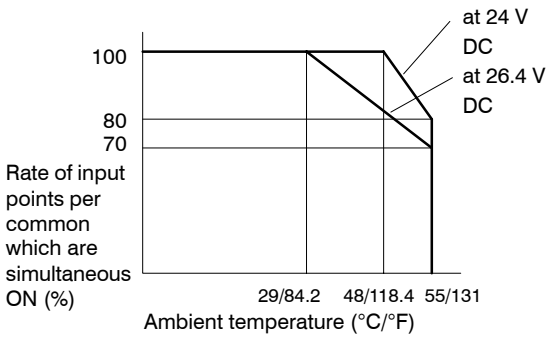
☞ **Notes**

- **COM terminals for I and II are internally connected.**
- **COM terminals for III and IV are internally connected.**
- **For more information regarding the applicable connectors and terminals, refer to section 4.4.**

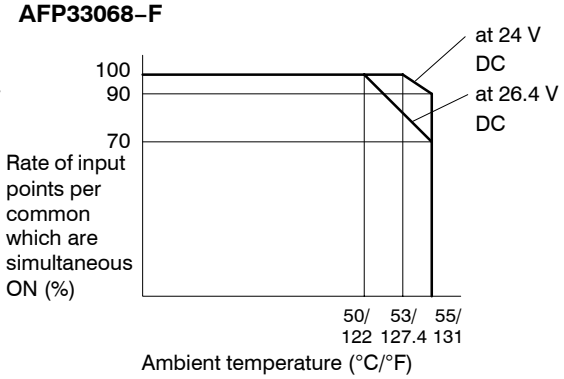
2.9.4.4 Limitations on Number of Simultaneous Input ON Points

Keep the rate of input points per common which are simultaneously ON within the following range as determined by the temperature.

AFP33028–F



AFP33068–F



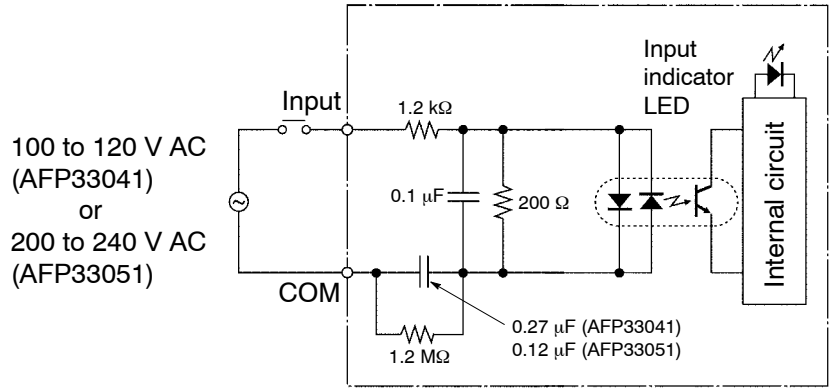
2.9.5 8-point Type AC Input Units

2.9.5.1 Specifications

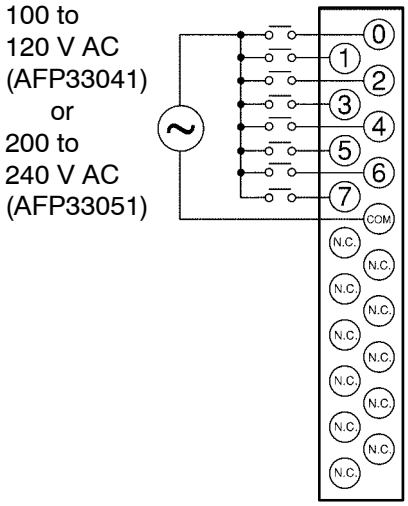
Item		Description	
Order number		AFP33041	AFP33051
Rated input voltage		100 to 120 V AC	200 to 240 V AC
Rated input current		approx. 10 mA (at 100 V AC)	approx. 10 mA (at 200 V AC)
Input impedance		approx. 10 k Ω	approx. 20 k Ω
Input voltage range		85 to 132 V AC (max. input current: 20 mA or less)	170 to 264 V AC (max. input current: 20 mA or less)
Min. ON voltage/ Min. ON current		80 V/6 mA	160 V/6 mA
Max. OFF voltage/ Max. OFF current		30 V/3 mA	50 V/3 mA
Response time	**OFF → ON**	15 ms or less	
	ON → OFF	30 ms or less	
Internal current consumption (at 5 V DC)		60 mA or less	
Input points per common		8 points/common	
Connection method		terminal block (M 3.5 screw)	
Weight		approx. 350 g/12.346 oz	

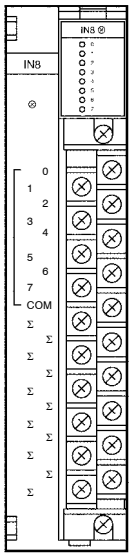
2.9.5.2 Internal Circuit Diagram

AFP33041/AFP33051



2.9.5.3 Pin Layout of Terminal Block





☞ **Note**

For more information regarding the applicable pressure connection (crimp) terminals and wiring, refer to section 4.5.

2.9.6 16-point Type AC Input Units

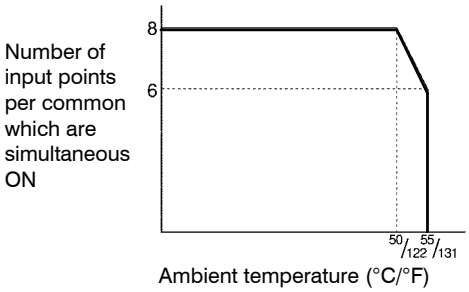
2.9.6.1 Specifications

Item		Description	
Order number		AFP33043	AFP33053
Rated input voltage		100 to 120 V AC	200 to 240 V AC
Rated input current		approx. 10 mA (at 100 V AC)	approx. 10 mA (at 200 V AC)
Input impedance		approx. 10 k Ω	approx. 20 k Ω
Input voltage range		85 to 132 V AC (max. input current: 20 mA or less)	170 to 264 V AC (max. input current: 20 mA or less)
Min. ON voltage/ Min. ON current		80 V/6 mA	160 V/6 mA
Max. OFF voltage/ Max. OFF current		30 V/3 mA	50 V/3 mA
Response time	**OFF → ON**	15 ms or less	
	ON → OFF	30 ms or less	
Internal current consumption (at 5 V DC)		60 mA or less	
Input points per common		8 points/common	
Connection method		terminal block (M 3.5 screw)	
Weight		approx. 350 g/12.346 oz	

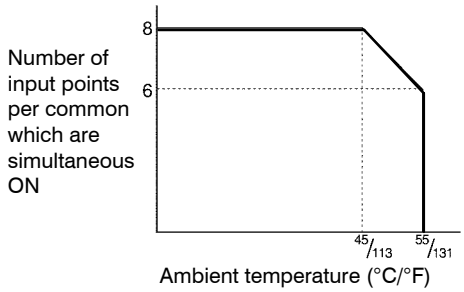
Limitations on Number of Simultaneous Input ON Points

Keep the number of input points per common which are simultaneously ON within the following range as determined by the ambient temperature.

AFP33043

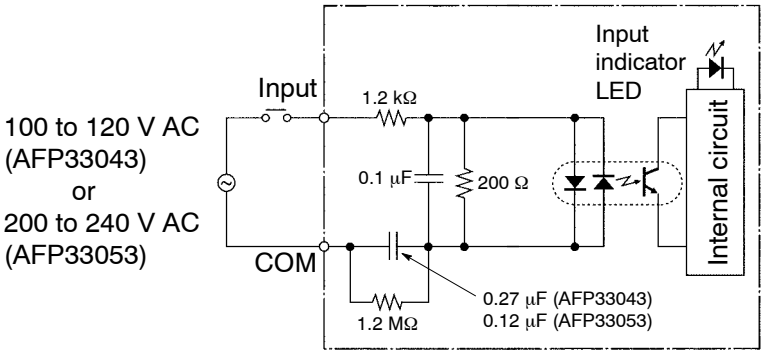


AFP33053



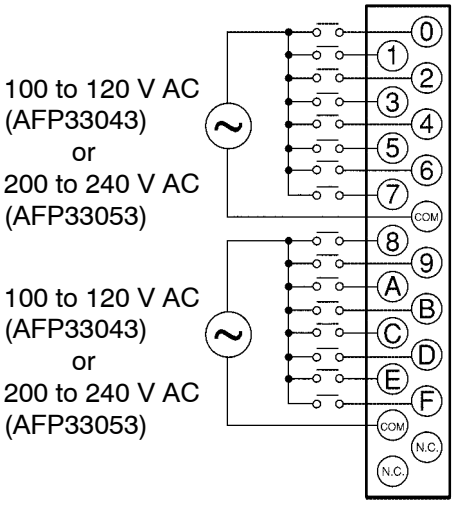
2.9.6.2 Internal Circuit Diagram

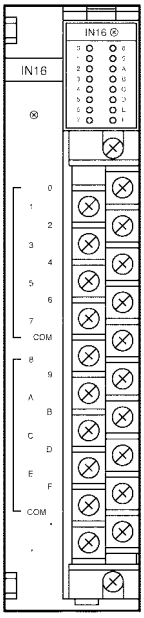
AFP33043/AFP33053



2.9.6.3 Pin Layout of Terminal Block

AFP33043/AFP33053





☞ **Note**

For more information regarding the applicable pressure connection (crimp) terminals and wiring, refer to section 4.5.

2.10 Output Units Specifications

2.10.1 16-point Type Relay Output Units

2.10.1.1 Specifications

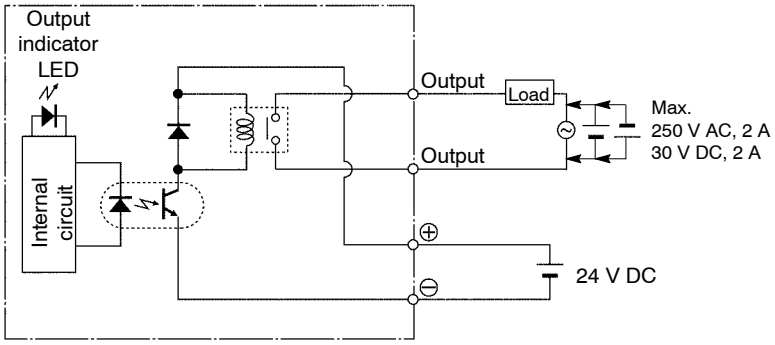
Item		Description
Order number		AFP33103−F/AFP33203−F
Rated control capacity (*Note)		2 A 250 V AC (5 A/common)/2 A 30 V DC (5 A/common)
Response time	**OFF → ON**	10 ms or less
	ON → OFF	8 ms or less
Life time	**Mechanical**	20,000,000 operations or more
	Electrical	100, 000 operations or more
Internal current consumption (at 5 V DC)		150 mA or less
Power supply for driving internal circuit	**Voltage**	24 V DC ± 10% (21.6 to 26.4 V DC)
	Current	160 mA or less
Surge absorber		none
Relay socket		AFP33103−F: without relay socket AFP33203−F: with relay socket
Output points per common		8 points/common
Connection method		terminal block (M 3.5 screw)
Weight		approx. 400 g/14.110 oz

☞ **Note**

Resistance load

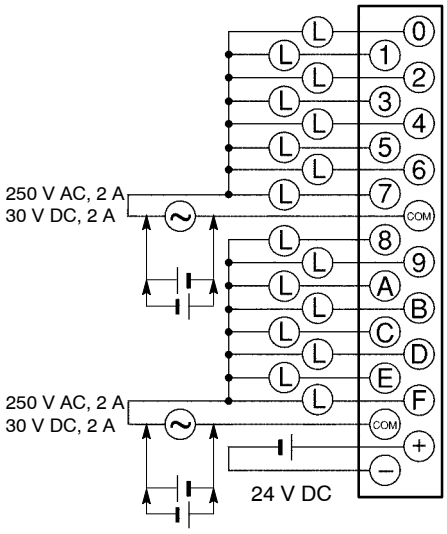
2.10.1.2 Internal Circuit Diagram

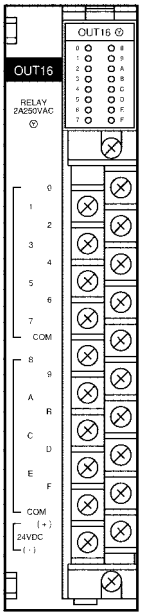
AFP33103−F/AFP33203−F



2.10.1.3 Pin Layout of Terminal Block

AFP33103−F/AFP33203−F





☞ **Note**

For more information regarding the applicable pressure connection (crimp) terminals and wiring, refer to section 4.5.

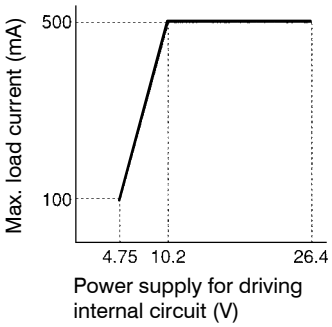
2.10.2 16-point Type Output Unit–Transistor NPN

2.10.2.1 Specifications

Item		Description
Order number		AFP33483–F
Rated load voltage		5 to 24 V DC
Load voltage range		4.75 to 26.4 V DC
Maximum load current (* Note)		0.5 A (at 12 to 24 V DC), 0.1 A (at 5 V DC)
Maximum surge current		3 A, 10 ms or less
OFF state leakage current		100 μA or less
ON state maximum voltage drop		0.5 V or less
Response time	**OFF → ON**	0.1 ms or less
	ON → OFF	0.3 ms or less
Internal current consumption (at 5 V DC)		100 mA or less
Power supply for driving internal circuit	**Voltage**	4.75 to 26.4 V DC (* Note)
	Current	100 mA (at 24 V DC)
Surge absorber		zener diode
Fuse ratings		5 A (AFP88042)
Output points per common		8 points/common
Connection method		terminal block (M 3.5 screw)
Weight		approx. 350 g/12.346 oz

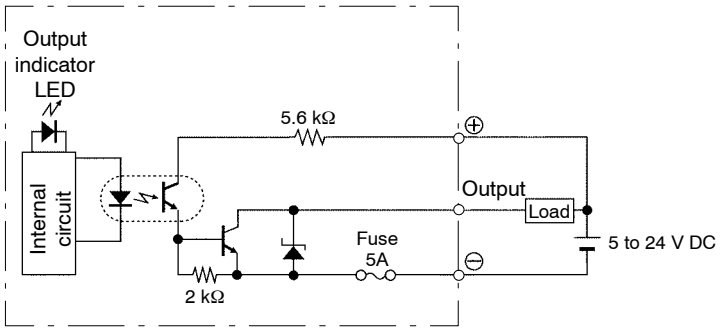
☞ **Note**

The load current will vary depending on the power supply for driving the internal circuit. Adjust the load current referring to the following range.



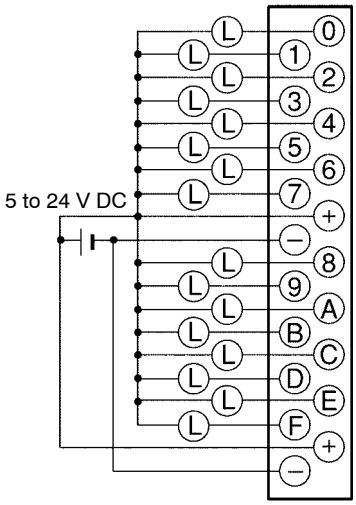
2.10.2.2 Internal Circuit Diagram

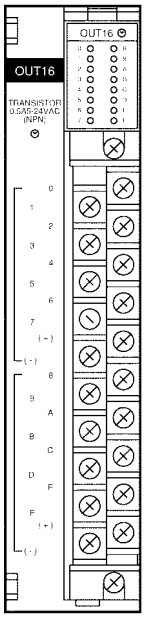
AFP33483–F



2.10.2.3 Pin Layout of Terminal Block

AFP33483–F





☞ Note

For more information regarding the applicable pressure connection (crimp) terminals and wiring, refer to section 4.5.

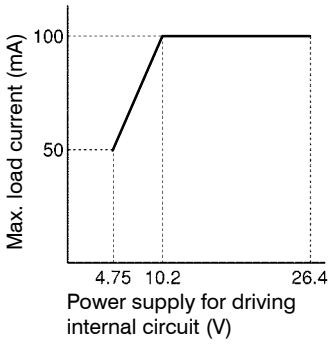
2.10.3 32-point Type Output Unit–Transistor NPN

2.10.3.1 Specifications

Item		Description
Order number		AFP33484–F
Rated load voltage		5 to 24 V DC
Load voltage range		4.75 to 26.4 V DC
Maximum load current (* Note)		0.1 A (at 12 to 24 V DC), 50 mA (at 5V DC)
Maximum surge current		0.3 A
OFF state leakage current		100 μA or less
ON state maximum voltage drop		0.5 V or less
Response time	**OFF → ON**	0.1 ms or less
	ON → OFF	0.3 ms or less
Internal current consumption (at 5 V DC)		160 mA or less
Power supply for driving internal circuit	**Voltage**	4.75 to 26.4 V DC (* Note)
	Current	100 mA (at 24 V DC)
Surge absorber		zener diode
Fuse ratings		none
Output points per common		16 points/common
Connection method		two 20-pin connectors
Weight		approx. 400 g/14.110 oz

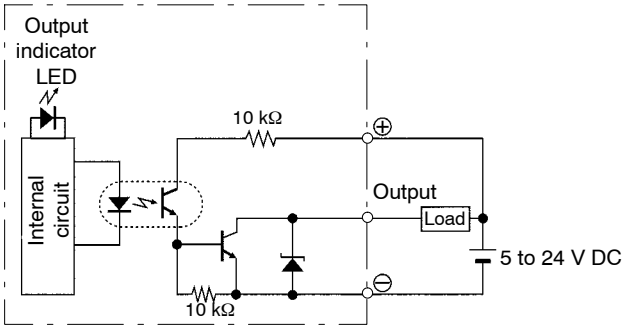
☞ **Note**

The load current will vary depending on the power supply for driving the internal circuit. Adjust the load current referring to the following range.



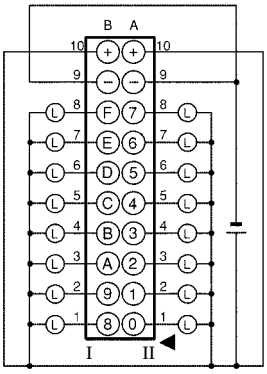
2.10.3.2 Internal Circuit Diagram

AFP33484−F



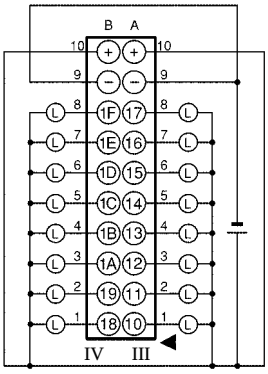
2.10.3.3 Pin Layout of Connector

Pin layout of
first 16 points

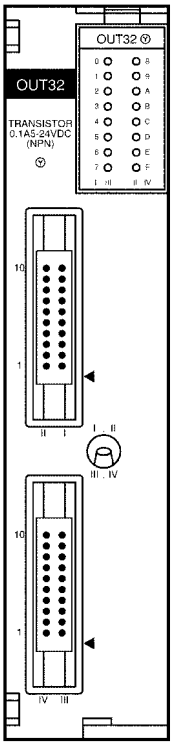


5 to 24 V DC

Pin layout of
last 16 points



5 to 24 V DC



☞ **Notes**

- **Although ⊕ (10A, 10B) and ⊖ (9A, 9B) terminals are connected with the same connector. It is recommended that they also be connected externally.**
- **For more information regarding the applicable connectors and terminals, refer to section 4.4.**

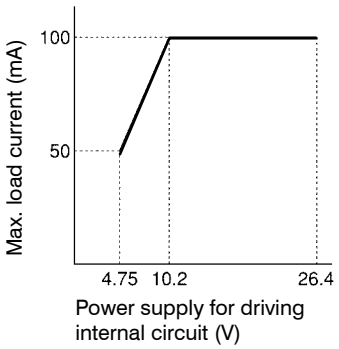
2.10.4 64-point Type Output Unit–Transistor NPN

2.10.4.1 Specifications

Item		Description
Order number		AFP33487–F
Rated load voltage		5 to 24 V DC
Load voltage range		4.75 to 26.4 V DC
Maximum load current (* Note)		0.1 A (at 12 to 24 V DC), 50 mA (at 5 V DC)
Maximum surge current		0.3 A
OFF state leakage current		100 μA or less
ON state maximum voltage drop		0.5 V or less
Response time	**OFF → ON**	0.1 ms or less
	ON → OFF	0.3 ms or less
Internal current consumption (at 5 V DC)		250 mA or less
Surge absorber		zener diode
Fuse ratings		none
Output points per common		32 points/common
Connection method		two 40-pin connectors
Weight		approx. 400 g/14.110 oz

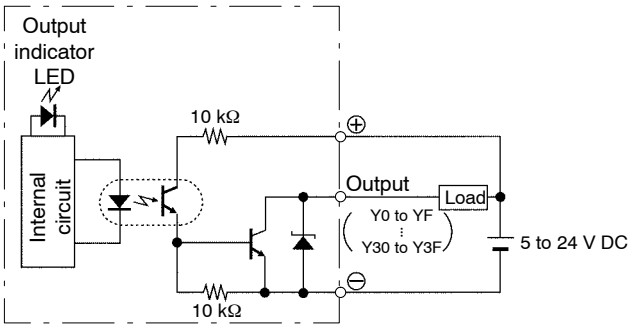
☞ **Note**

The load current will vary depending on the power supply for driving the internal circuit. Adjust the load current referring to the following range.



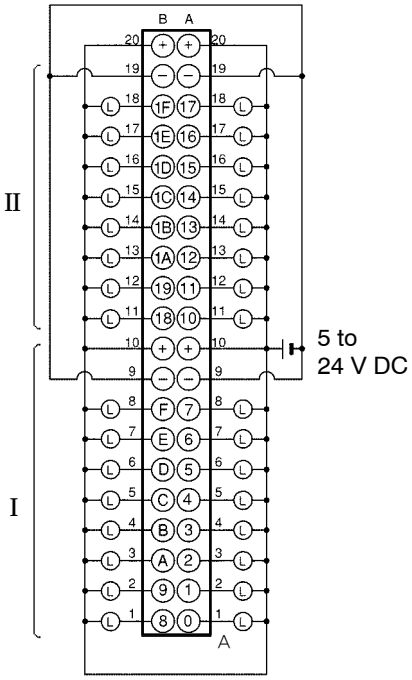
2.10.4.2 Internal Circuit Diagram

AFP33487–F

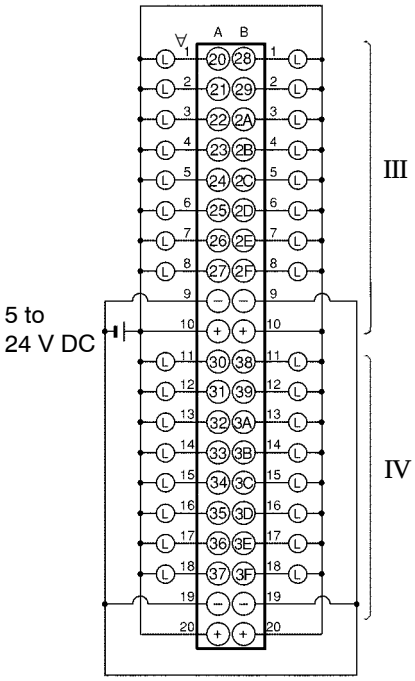


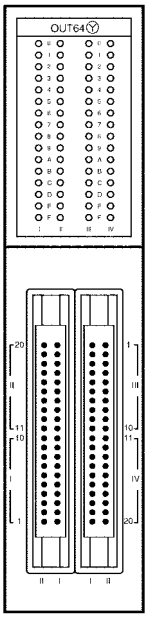
2.10.4.3 Pin Layout of Connector

Pin layout of first 32 points



Pin layout of last 32 points





☞ **Notes**

- **Although ⊕ and ⊖ pins are connected with the same connector. It is recommended that they also be connected externally.**
- **For more information regarding the applicable connectors and terminals, refer to section 4.4.**

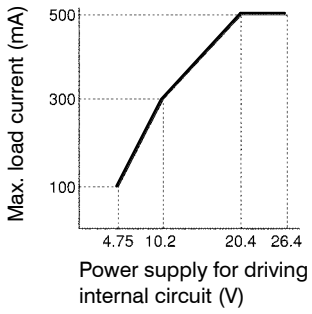
2.10.5 16-point Type Output Unit–Transistor PNP

2.10.5.1 Specifications

Item		Description
Order number		AFP33583–F
Rated load voltage		5 to 24 V DC
Load voltage range		4.75 to 26.4 V DC
Maximum load current (* Note)		0.5 A (at 24 V DC), 0.3 A (at 12 V DC), 0.1 A (at 5 V DC)
Maximum surge current		5 A, 100 ms or less
OFF state leakage current		100 μA or less
ON state maximum voltage drop		0.5 V or less
Response time	**OFF → ON**	0.1 ms or less
	ON → OFF	0.3 ms or less
Internal current consumption (at 5 V DC)		120 mA or less
Power supply for driving internal circuit	**Voltage**	4.75 to 26.4 V DC (* Note.)
	Current	200 mA (at 24 V DC)
Surge absorber		zener diode
Fuse ratings		5 A (1 piece/common)
Output points per common		8 points/common
Connection method		terminal block (M 3.5 screw)
Weight		approx. 350 g/12.346 oz

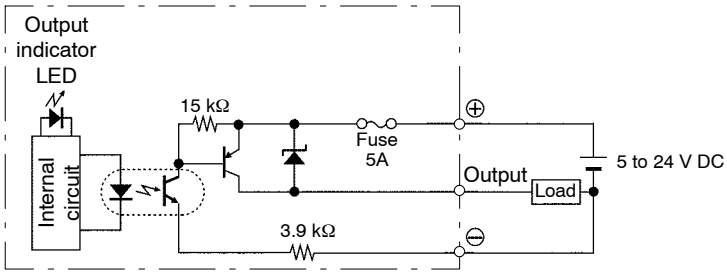
☞ **Note**

The load current will vary depending on the power supply for driving the internal circuit. Adjust the load current referring to the following range.



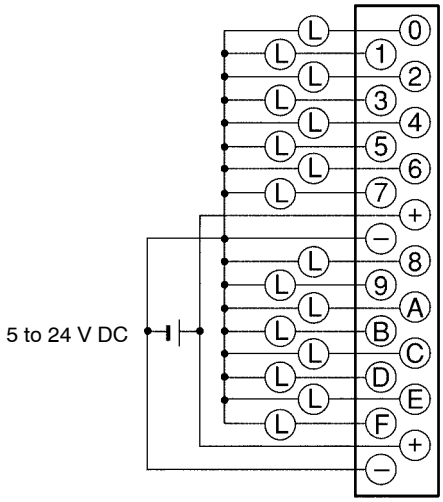
2.10.5.2 Internal Circuit Diagram

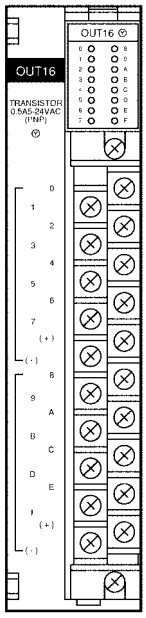
AFP33583−F



2.10.5.3 Pin Layout of Terminal Block

AFP33583−F





☞ **Note**

For more information regarding the applicable pressure connection (crimp) terminals and wiring, refer to section 4.5.

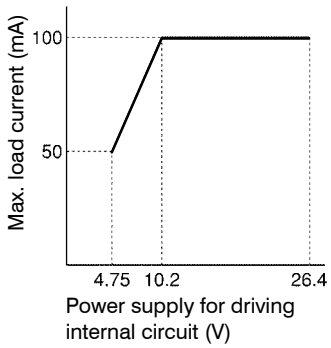
2.10.6 32-point type Output Unit–Transistor PNP

2.10.6.1 Specifications

Item		Description
Order number		AFP33584–F
Rated load voltage		5 to 24 V DC
Load voltage range		4.75 to 26.4 V DC
Maximum load current (* Note)		0.1 A (at 12 to 24 V DC)
Maximum surge current		0.3 A
OFF state leakage current		100 μA or less
ON state maximum voltage drop		0.5 V or less
Response time	**OFF → ON**	0.1 ms or less
	ON → OFF	0.3 ms or less
Internal current consumption (at 5 V DC)		160 mA or less
Power supply for driving internal circuit	**Voltage**	4.75 to 26.4 V DC (* Note)
	Current	100 mA (at 24 V DC)
Surge absorber		zener diode
Fuse ratings		none
Output points per common		16 points/common
Connection method		two 20-pin connectors
Weight		approx. 400 g/14.110 oz

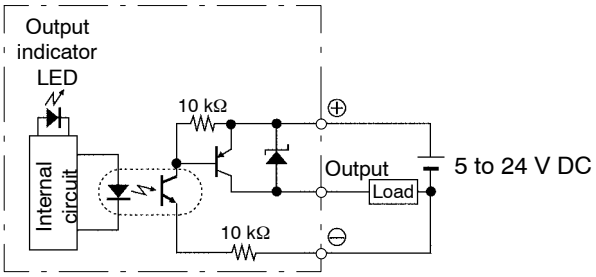
☞ **Note**

The load current will vary depending on the power supply for driving the internal circuit. Adjust the load current referring to the following range.



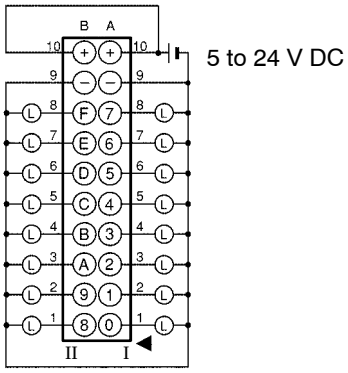
2.10.6.2 Internal Circuit Diagram

AFP33584−F

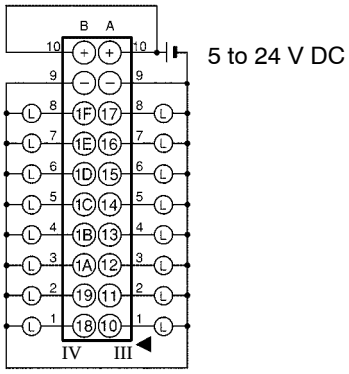


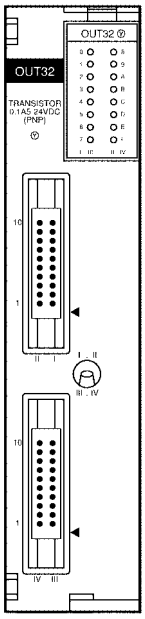
2.10.6.3 Pin Layout of Connector

Pin layout of
first 16 points



Pin layout of
last 16 points





☞ **Notes**

- **Although ⊕ pins for I, II, III, IV and ⊖ pins for I, II, III, IV are internally connected.**
  It is recommended that they also be connected externally.
- **For more information regarding the applicable connectors and terminals, refer to section 4.4.**

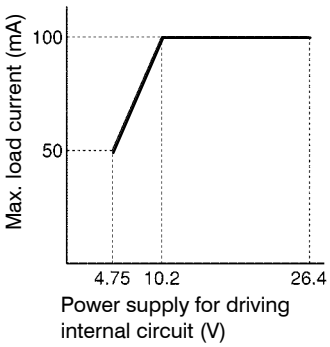
2.10.7 64-point Type Output Unit–Transistor PNP

2.10.7.1 Specifications

Item		Description
Order number		AFP33587–F
Rated load voltage		5 to 24 V DC
Load voltage range		4.75 to 26.4 V DC
Maximum load current (* Note)		0.1 A (at 12 to 24 V DC), 50 mA (at 5 V DC)
Maximum surge current		0.3 A
OFF state leakage current		100 μA or less
ON state maximum voltage drop		0.5 V or less
Response time	**OFF → ON**	0.1 ms or less
	ON → OFF	0.3 ms or less
Internal current consumption (at 5 V DC)		250 mA or less
Surge absorber		zener diode
Fuse ratings		none
Output points per common		32 points/common
Connection method		two 40-pin connectors
Weight		approx. 400 g/14.110 oz

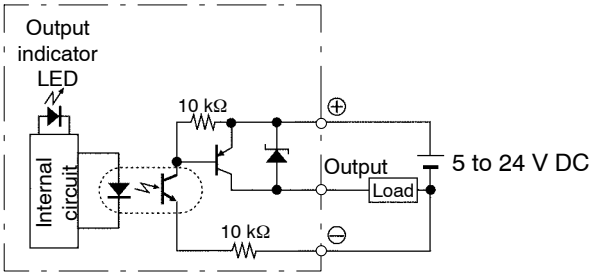
☞ **Note**

The load current will vary depending on the power supply for driving the internal circuit. Adjust the load current referring to the following range.



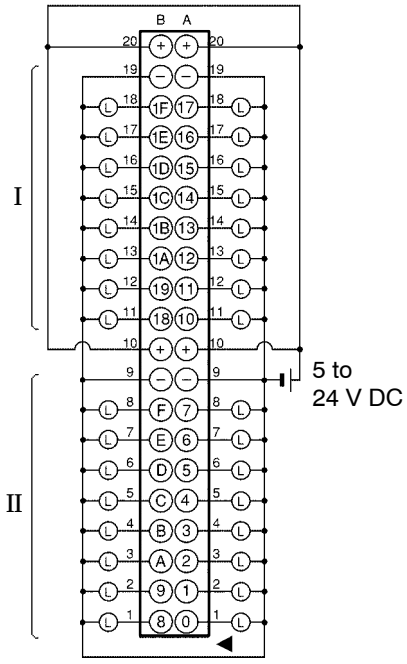
2.10.7.2 Internal Circuit Diagram

AFP33587−F

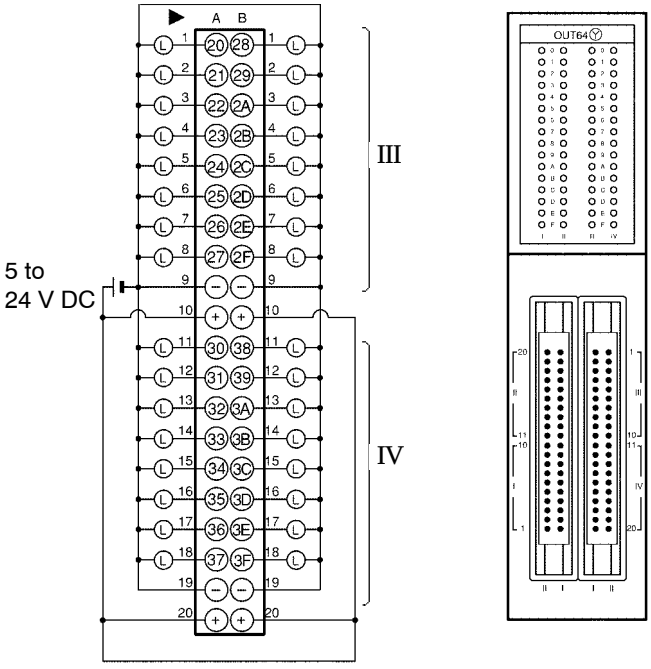


2.10.7.3 Pin Layout of Connector

Pin layout of first 32 points



Pin layout of last 32 points



☞ **Notes**

- **Although ⊕ pins and ⊖ pins are internally connected. It is recommended that they also be connected externally.**
- **For more information regarding the applicable connectors and terminals, refer to section 4.4.**

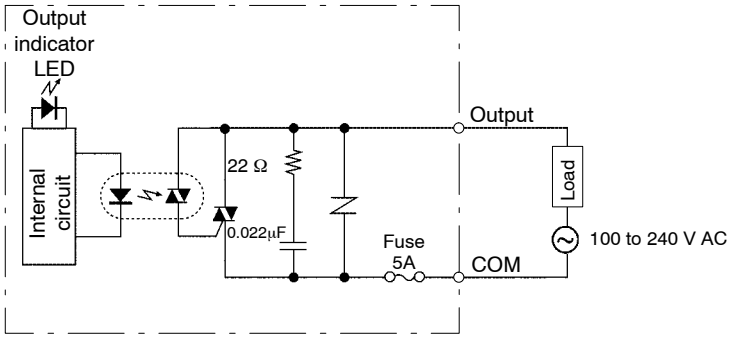
2.10.8 16-point Type Triac Output Unit

2.10.8.1 Specifications

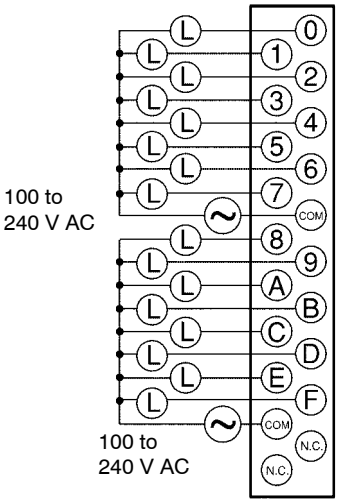
Item		Description
Order number		AFP33703
Rated load voltage		100 to 240 V AC, 50/60 Hz
Load voltage range		85 to 264 V AC
Maximum load current		0.5 A/point, 2 A/common
Maximum surge current		15 A, 100 ms or less
Minimum load current		25 mA
OFF state leakage current		3 mA or less (at 240 V AC)
ON state maximum voltage drop		2.5 V or less (0.1 A or less) 1.5 V or less (0.1 A to 0.5 A)
Response time	**OFF → ON**	1 ms or less
	ON → OFF	0.5 cycle + 1 ms or less
Internal current consumption (at 5 V DC)		200 mA or less
Surge absorber		varistor
Fuse ratings		5 A (1 piece/common)
Output points per common		8 points/common
Connection method		terminal block (M 3.5 screw)
Weight		approx. 400 g/14.110 oz

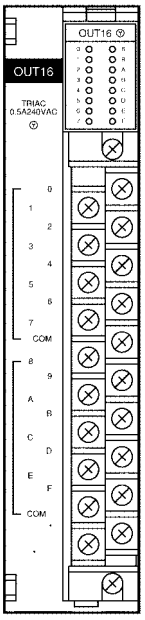
2.10.8.2 Internal Circuit Diagram

AFP33703



2.10.8.3 Pin Layout of Terminal Block





☞ Note

For more information regarding the applicable pressure connection (crimp) terminals and wiring, refer to section 4.5.

2.11 I/O Mixed Units Specifications

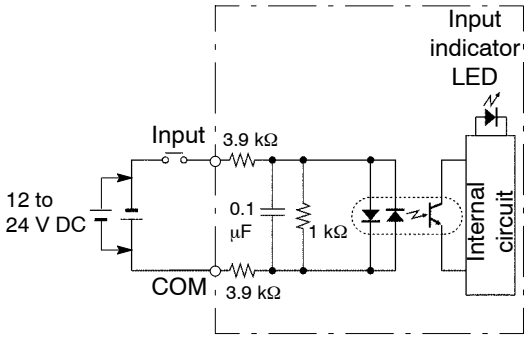
2.11.1 64–point Type I/O Mixed Unit–DC Input/Transistor NPN

2.11.1.1 Specifications

Item			Description
Order number			AFP33428–F
Input	**Number of input points**		32 points
	Rated input voltage		12 to 24 V DC
	Rated input current		approx. 6.2 mA (at 24 V DC)
	Input impedance		approx. 3.9 k Ω
	Input voltage range		10.2 to 26.4 V DC
	Min. ON voltage/Min. ON current		9.6 V/3 mA
	Max. OFF voltage/Max. OFF current		2.5 V/1 mA
	Response time	**OFF → ON**	0.1 ms or less
		ON → OFF	0.3 ms or less
	Input points per common		32 points/common Either the positive or negative of the input power supply can be connected to COM (common) terminal.
Output	**Number of output points**		32 points
	Rated load voltage		5 to 24 V DC
	Load voltage range		4.75 to 26.4 V DC
	Maximum load current		0.1 A (at 12 to 24 V DC), 50 mA (at 5 V DC)
	Maximum surge current		0.3 A or less
	OFF state leakage current		100 μA or less
	ON state maximum voltage drop		0.5 V or less
	Response time	**OFF → ON**	0.1 ms or less
		ON → OFF	0.3 ms or less
	Power supply for driving internal circuit	**Voltage**	4.75 to 26.4 V DC
		Current	100 mA (at 24 V DC)
	Surge absorber		zener diode
	Fuse ratings		none
	Output points per common		32 points/common
Internal current consumption (at 5 V DC)			230 mA or less
Connection method			two 40-pin connectors
Weight			approx. 400 g/14.110 oz

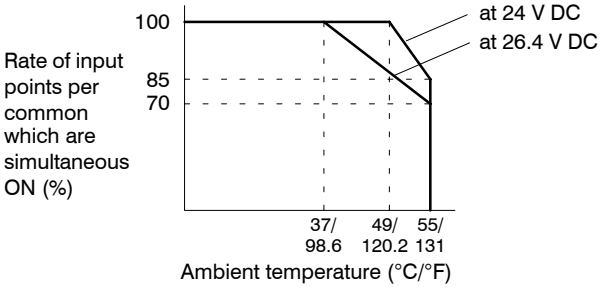
2.11.1.2 Internal Circuit Diagram

AFP33428–F
Input section (left side connector)

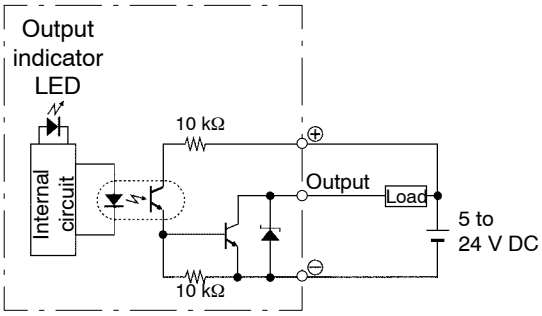


☞ **Note**

Keep the rate of input points per common which are simultaneously ON within the following range as determined by the temperature.



Output section (right side connector)



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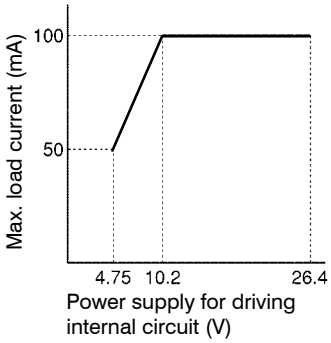
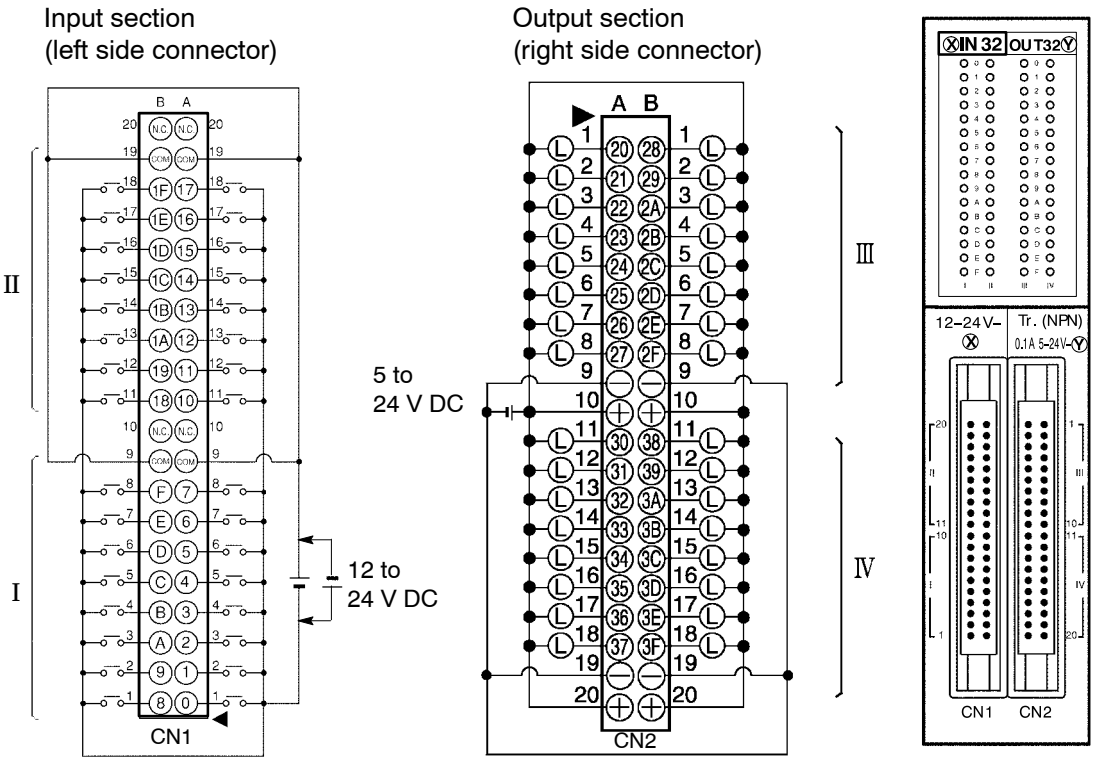
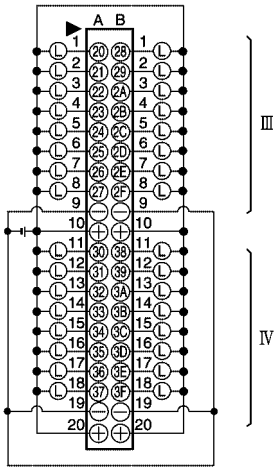
☞ **Note**

The load current will vary depending on the power supply for driving the internal circuit. Adjust the load current referring to the following range.



2.11.1.3 Pin Layout of Connector





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☞ Notes

- **COM pins for I and for II are internally connected.**
- **Although ⊕ pins and ⊖ pins for III and for IV are internally connected. It is recommended that they also be connected externally.**
- **For more information regarding the applicable connectors and terminals, refer to section 4.4.**

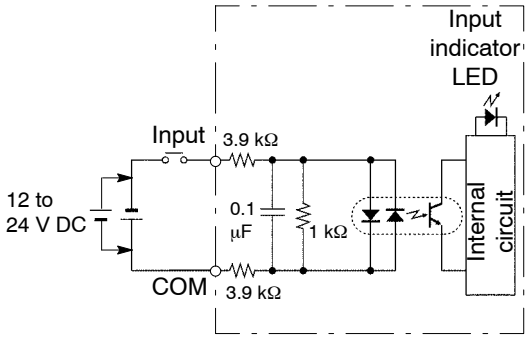
2.11.2 64–point Type I/O Mixed Unit–DC Input/Transistor PNP

2.11.2.1 Specifications

Item			Description
Order number			AFP33528–F
Input	**Number of input points**		32 points
	Rated input voltage		12 to 24 V DC
	Rated input current		approx. 6.2 mA (at 24 V DC)
	Input impedance		approx. 3.9 k Ω
	Input voltage range		10.2 to 26.4 V DC
	Min. ON voltage/Min. ON current		9.6 V/3 mA
	Max. OFF voltage/Max. OFF current		2.5 V/1 mA
	Response time	**OFF → ON**	0.1 ms or less
		ON → OFF	0.3 ms or less
	Input points per common		32 points/common Either the positive or negative of the input power supply can be connected to COM (common) terminal.
Output	**Number of output points**		32 points
	Rated load voltage		5 to 24 V DC
	Load voltage range		4.75 to 26.4 V DC
	Maximum load current		0.1 A (at 12 to 24 V DC), 50 mA (at 5 V DC)
	Maximum surge current		0.3 A or less
	OFF state leakage current		100 μA or less
	ON state maximum voltage drop		0.5 V or less
	Response time	**OFF → ON**	0.1 ms or less
		ON → OFF	0.3 ms or less
	Power supply for driving internal circuit	**Voltage**	4.75 to 26.4 V DC
		Current	100 mA (at 24 V DC)
	Surge absorber		zener diode
	Fuse ratings		none
	Output points per common		32 points/common
Internal current consumption (at 5 V DC)			230 mA or less
Connection method			two 40-pin connectors
Weight			approx. 400 g/14.110 oz

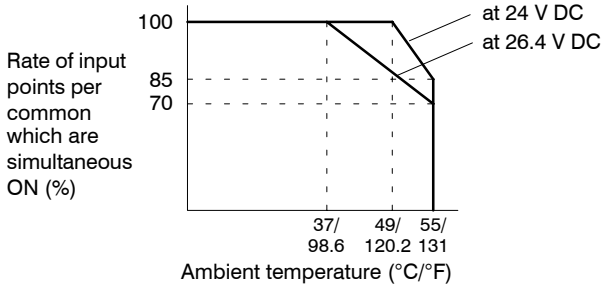
2.11.2.2 Internal Circuit Diagram

AFP33528−F
Input section (left side connector)

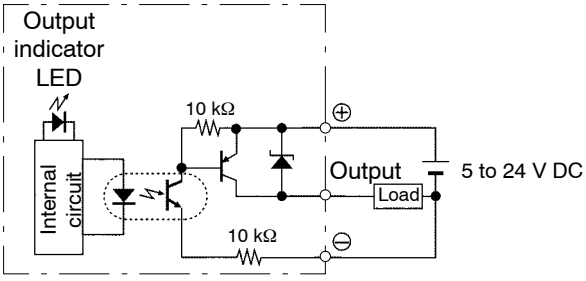


☞ **Note**

Keep the rate of input points per common which are simultaneously ON within the following range as determined by the temperature.



Output section (right side connector)



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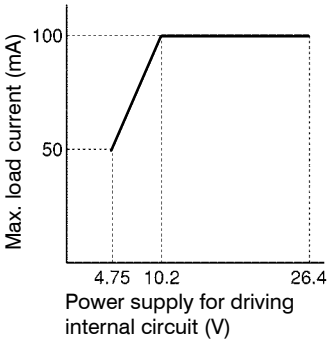
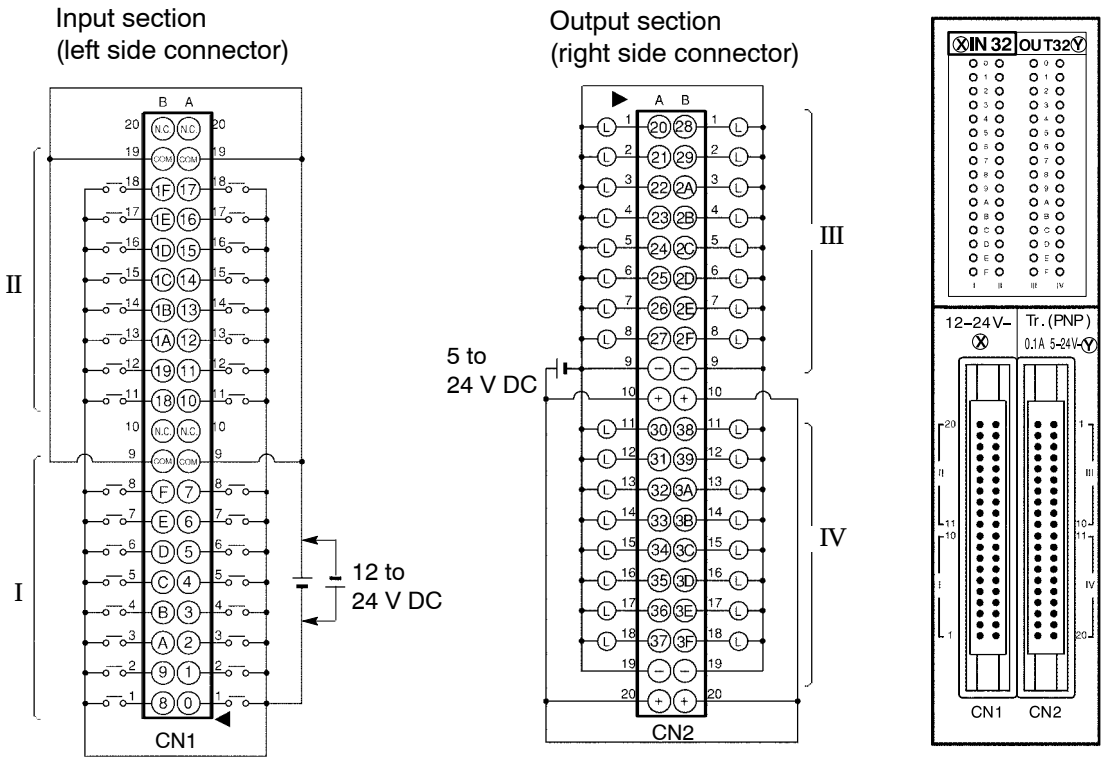
☞ **Note**

The load current will vary depending on the power supply for driving the internal circuit. Adjust the load current referring to the following range.



2.11.2.3 Pin Layout of Connector



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☞ Notes

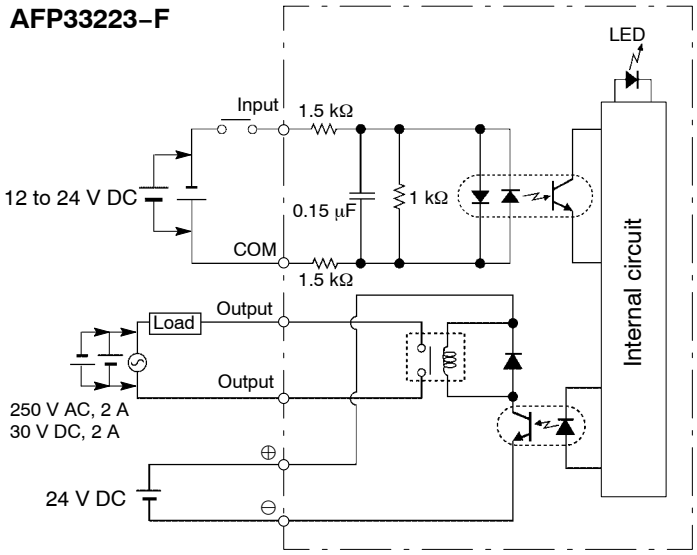
- **COM pins for I and for II are internally connected.**
- **Although ⊕ pins and ⊖ pins for III and for IV are internally connected. It is recommended that they also be connected externally.**
- **For more information regarding the applicable connectors and terminals, refer to section 4.4.**

2.11.3 16–point Type I/O Mixed Unit–DC Input/Relay Output

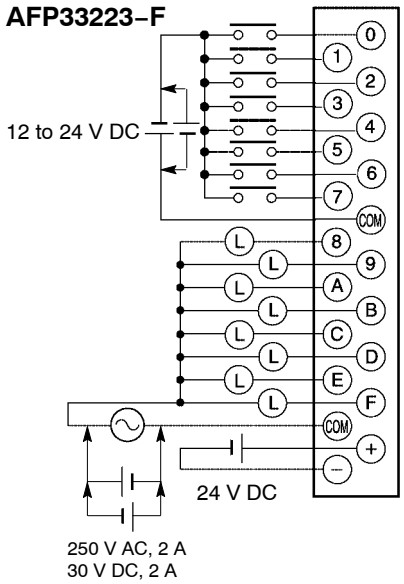
2.11.3.1 Specifications

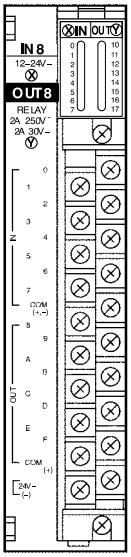
Item			Description
Order number			AFP33223–F
Input	**Number of input points**		8 points
	Rated input voltage		12 to 24 V DC
	Rated input current		approx. 8 mA (at 24 V DC)
	Input impedance		approx. 3 k Ω
	Input voltage range		10.2 to 26.4 V DC (max. input current: 10 mA)
	Min. ON voltage/Min. ON current		9.6 V/4 mA
	Max. OFF voltage/Max. OFF current		2.5 V/1 mA
	Response time	**OFF → ON**	1.5 ms or less
		ON → OFF	2.0 ms or less
	Input points per common		8 points/common Either the positive or negative of the input power supply can be connected to COM (common) terminal.
Output	**Number of output points**		8 points
	Rated control capacity		2 A 250 V AC (5 A/common), 2 A 30 V DC (5 A/common)
	Response time	**OFF → ON**	10 ms or less
		ON → OFF	8 ms or less
	Life time	**Mechanical**	20,000,000 operations or more
		Electrical	100,000 operations or more
	Power supply for driving internal circuit	**Voltage**	24 V DC ± 10% (21.6 to 26.4 V DC)
		Current	80 mA or less
	Surge absorber		none
	Relay socket		with relay socket
	Output points per common		8 points/common
Internal current consumption (at 5 V DC)			150 mA or less
Connection method			terminal block (M 3.5 screw)
Weight			approx. 400 g/14.110 oz

2.11.3.2 Internal Circuit Diagram



2.11.3.3 Pin Layout of Terminal Block





☞ Note

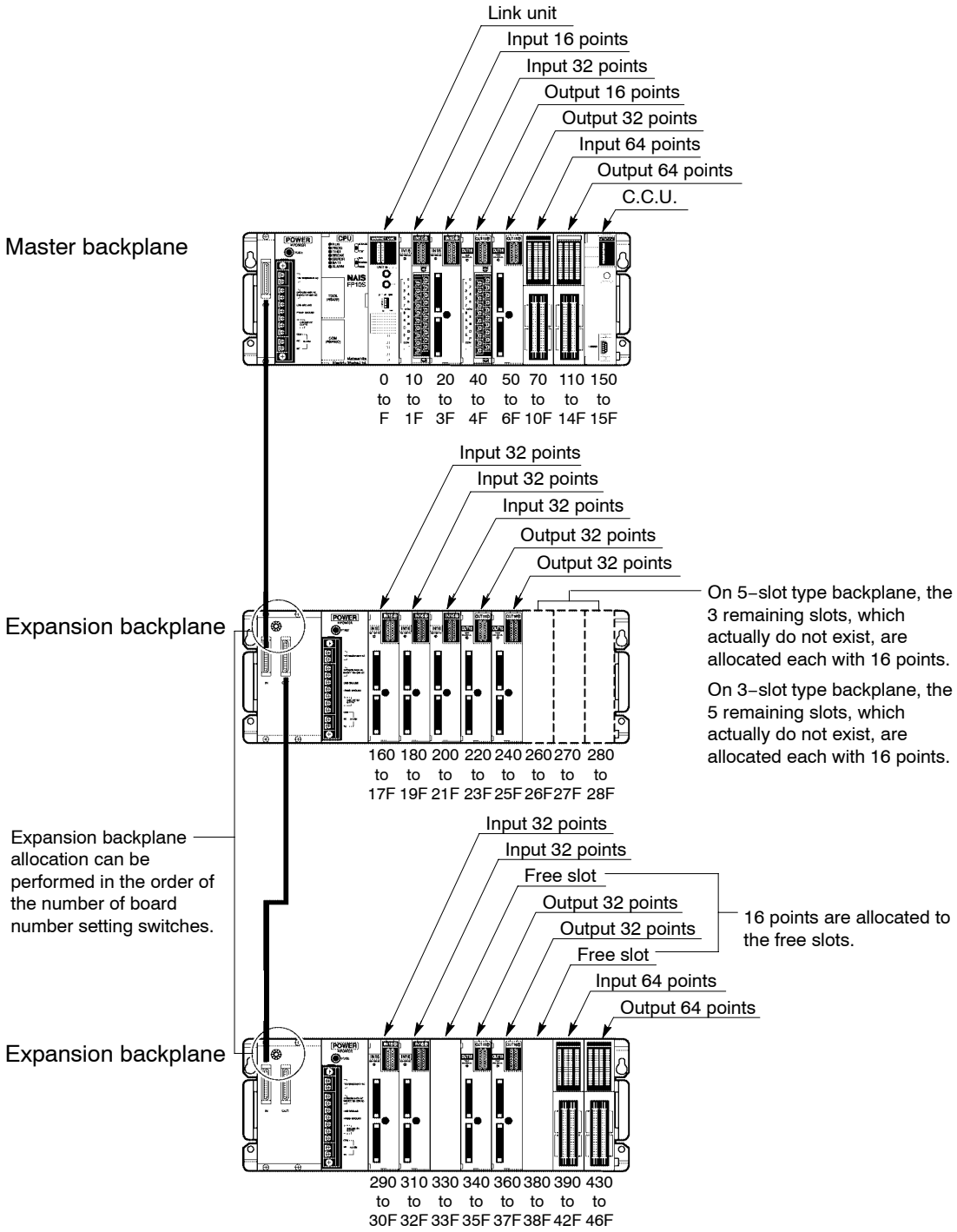
For more information regarding the applicable pressure connection (crimp) terminals and wiring, refer to section 4.5.

Chapter 3

I/O Allocation

3.1 Fundamentals of I/O Allocation (Automatic Allocation)

3.1.1 Example of Automatic Allocation

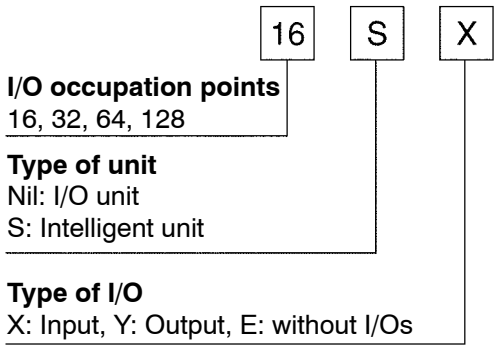


3.1.2 Using Automatic Allocation

The I/O number is determined by the unit installation location and allocated in order starting from the left side (slot 0) of the master backplane.

I/O points are allocated for each unit according to its own I/O occupation (* section 3.4). In the table of section 3.4, the occupied points are expressed in the following fashion for convenience.

How to express the occupied points

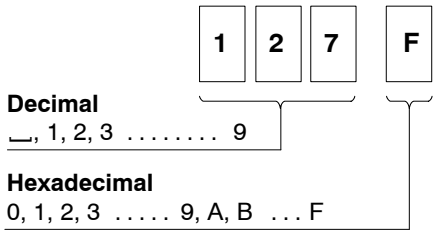


16 points are allocated for the free slot.

All backplanes, including 3- and 5-slot types, are regarded as 8-slot types, and slots which do not actually exist are regarded as open slots.
On 5–slot type backplane, the 3 remaining slots, which actually do not exist, are allocated each with 16 points.
On 3–slot type backplane, the 5 remaining slots, which actually do not exist, are allocated each with 16 points.
Expansion backplane allocation can be performed in the order of the numbers of the board number setting switches.

How to count the I/O numbers (relay numbers)
Since I/O number are handled in units of 16 points, they are expressed as a combination of decimal and hexadecimal numbers as shown below.

<Example>



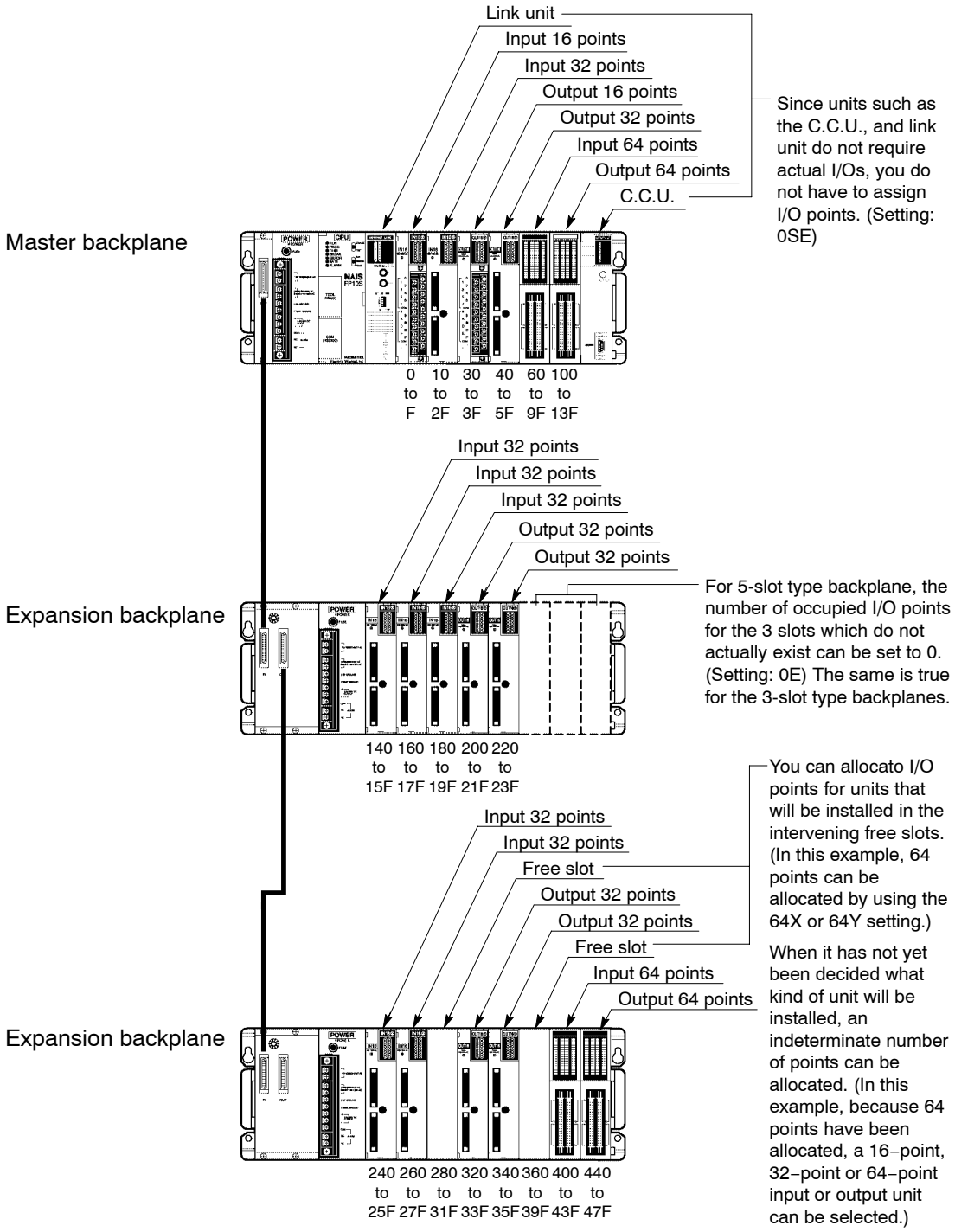
3.1.3 Procedure for Automatic Allocation

Automatic allocation is performed automatically when the power supply is turned ON.

If you have already set arbitrary allocation (* section 3.2) or the I/O mount allocation (* section 3.3), the I/O allocation will be performed according to those settings. If you want to return to automatic allocation, initialize the system register (* section 3.3.1.2).

3.2 Arbitrary Allocation With NPST−GR

3.2.1 Example of Arbitrary Allocation With NPST−GR



3.2.2 Using Arbitrary Allocation

You have the following advantages when you use the NPST−GR software to perform arbitrary allocation.

For link unit and C.C.U. (computer communication unit), etc., that do not require actual I/Os, the number of I/O points can be set to 0, and the I/O numbers will be renumbered accordingly. (Use the NPST-GR setting: 0SE).

For the 5-slot type backplanes, the number of I/O points for the 3 slots which do not actually exist can be set to 0 and the I/O numbers will be renumbered accordingly.
For the 3-slot type backplanes, the number of I/O points for the 5 slots which do not actually exist can be set to 0 and the I/O numbers will be renumbered accordingly.
(Use the NPST-GR setting: 0E).

For free slots, I/O points can be allocated for I/O units that will be installed later. For example, if a 32-point or 64-point unit will be added in the future, the addition of the unit will not affect the I/O numbers for the subsequent units.

When there is a possibility that the number of I/O points will increase, but the type of unit has not yet been decided, an indeterminate number of points can be allocated.

In this example, because 64 points (64Y) have been allocated in the free slot, a 16−point, 32−point or 64−point output unit can be selected. The addition of the unit will not affect the I/O numbers for the subsequent units.

☞ **Note**

When arbitrary allocation is not used, I/Os will be allocated automatically according to the automatic allocation.

3.2.3 Procedure of Arbitrary Allocation

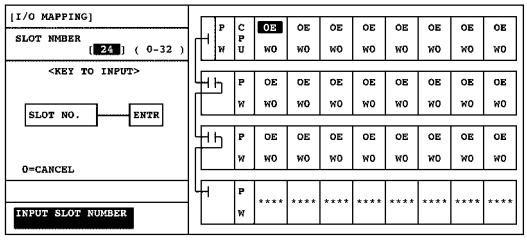
You can use the NPST−GR software. If you want to use NPST−GR software, read the NPST−GR manuals.

Procedure:

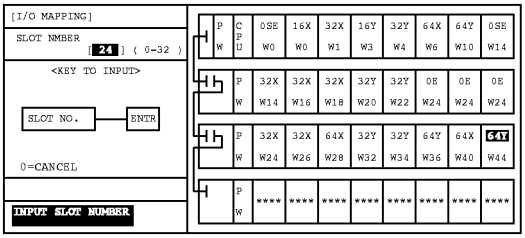
1. **Set the NPST−GR to OFFLINE mode.**
2. **Press the <ESC> key to display the “NPST MENU.” Select “ALLOCATE I/O MAP” from “PLC CONFIGURATION” of the menu and press the <ESC> key.**

<Settings for the example on page 3 − 6>

1. Set the number of slots to 24. (The slots will be set at 8 slots per one backplane.)



2. Allocations will be performed for each unit according to the settings.



3. After the allocations are completed, register the contents of allocation by pressing the <Ctrl> and <f1> keys simultaneously. The registered settings can be written to the FP3/FP10SH CPU together with the program.
   The system will operate according to the I/O allocation.

Writing contents of arbitrary allocation on the NPST−GR screen

1. Press the <ESC> key to display the “NPST MENU.”
2. Select “PROGRAM MANAGER” then “LOAD A PROGRAM TO PLC”, and press the <ESC> key. The program is transferred to the FP3/FP10SH CPU, and the contents of allocation are simultaneously written to the FP3/FP10SH CPU as part of its system register settings.

3.3 Registration of I/O Mount Allocation

3.3.1 Registration Method of Mount State

Registering with NPST-GR

Procedure:

1. **Set the mode selector of CPU to the PROG. mode and set the NPST−GR to online mode.**
2. **Press the <ESC> key to display the “NPST MENU.” Select “ALLOCATE I/O MAP” from the “PLC CONFIGURATION”, and press the <ENTER> key.**
3. **Then press <F10 (LD I/O)> key to register the current I/O mapping.**
4. **Verify that “OK? (Y/N)” appears, and then press the <Y> key. By selecting “Y” in the screen, the unit currently mounted is read to the NPST−GR screen, and the contents of allocation are recorded to the CPU at the same time. The contents recorded at this time are the same as the contents for automatic allocation.**

Registering with FP programmer II Ver.2

Perform the following key operations.
The contents recorded at this time are the same as the contents for automatic allocation.

3.3.1.1 Using Registration of I/O Allocation

The registration of I/O allocation refers to the registration of the I/O numbers assigned to each unit in the system registers of the CPU.

For automatic allocation (* section 3.1), the allocation depends on the state of the installed units when the power is turned ON. However, if the I/O allocations are registered, the I/O numbers will not be shifted even if there are mistakes in the installation of the units.

Arbitrary allocation (* section 3.2) is registered in the CPU at the same time the program is written, so there is no need for the registration operation.

☞ next page

☞ **Notes**

- **It is not absolutely necessary to perform the registration of I/O allocation. If the allocation is not registered, the system will operate according to the automatic allocations.**
- **If the I/O allocation is registered, correct operation will not be possible if units are changed or mount positions are changed after registration. Redo the registration if the installation conditions do match the contents of the registration.**

3.3.1.2 Clearing Registered Content

The registered content is cleared by initializing system register.

Note that the contents of all the system registers will be reset when you initialize system register.

Clearing content using NPST-GR

Procedure:

1. **Set the NPST−GR to ONLINE monitor.**
2. **Press the <ESC> key to display the “NPST MENU.” Select “SYSTEM REGISTER” from the “PLC CONFIGURATION” of the NPST menu, and press the <ENTER> key.**
3. **press <F2 (INT)> key.**
4. **Verify that “INITIALIZE? (Y/N)” is displayed, and press the <Y> key. The contents of the system register will be cleared.**

Clearing content using FP programmer

Perform the following key operations.

3.4 Table of I/O Occupied Points

Name				Order number	I/O occupied point
Input unit	DC input	16-point, terminal	12 to 24 V DC	AFP33023–F	16X
		32-point, connector	12 to 24 V DC	AFP33024–F	32X
			5 V DC	AFP33014–F	
		64-point, connector	12 to 24 V DC	AFP33027–F	64X
				AFP33028–F	
			24 V DC	AFP33068–F	
			5 V DC	AFP33017–F	
	AC input	8-point, terminal	100 to 120 V AC	AFP33041	16X
			200 to 240 V AC	AFP33051	
		16-point, terminal	100 to 120 V AC	AFP33043	16X
			200 to 240 V AC	AFP33053	
Output unit	Relay output	16-point, terminal	With relay socket	AFP33203–F	16Y
			Without relay socket	AFP33103–F	
	Transistor output	16-point, terminal	NPN open collector	AFP33483–F	16Y
			PNP open collector	AFP33583–F	
		32-point, connector	NPN open collector	AFP33484–F	32Y
			PNP open collector	AFP33584–F	
		64-point, connector	NPN open collector	AFP33487–F	64Y
			PNP open collector	AFP33587–F	
	Triac output	16-point, terminal		AFP33703	16Y
I/O mixed unit	DC input/ relay output type	16-point, terminal		AFP33223–F	16X 16Y
	DC input/ transistor (NPN) output	64-point, connector		AFP33428–F	32X 32Y
	DC input/ transistor (PNP) output	64-point, connector		AFP33528–F	32X 32Y

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3.4 Table of I/O Occupied Points

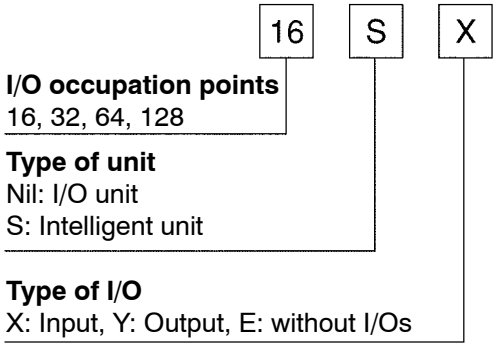
Name			Order number	I/O occupied point
A/D converter unit	**4-channel**	**Standard type**	AFP3400	16SX
	8-channel	**G-type**	AFP3402	16SE (0SE) **(* Note 1)**
			AFP3403	
			AFP3405	
	8-channel	**I-type**	AFP3406	
			AFP3407	
			AFP3408	
D/A converter unit	**2-channel**	**Standard type**	AFP3410	16SX
			AFP3411	
	2-channel	**I-type**	AFP3412	16SE (0SE) **(* Note 1)**
			AFP3413	
			AFP3416	
			AFP3417	
	4-channel	**I-type**	AFP3414	
			AFP3415	
			AFP3418	
			AFP3419	
R.T.D. input unit			AFP3420	16SX
Thermocouple input unit			AFP3421	16SX
Serial data unit			AFP3460	16SX 16SY
Data process unit			AFP3461	
High-speed counter unit		**1-channel type**	AFP3621	
		2-channel type	AFP3622	
Pulse output unit			AFP3480	16SX/16SY
Positioning unit E-type			AFP3431E	16SX/16SY
			AFP3432E	32SX/32SY
Positioning unit F-type			AFP3431	16SX 16SY
			AFP3434	
			AFP3432	32SX 32SY
			AFP3435	
			AFP3436	
Interrupt unit			AFP3452	16SX
MEWNET-TR transmitter master unit			AFP3750	0X to 128X 0Y to 128Y **(* Note 2)**
MEWNET-F master unit			AFP3742	16SE (0SE) **(* Note 1)**
MEWNET-W link unit			AFP3720	

☞ next page

Name	Order number	I/O occupied point
MEWNET-P link unit	AFP3710	16SE (0SE) **(* Note 1)**
C-NET link unit	AFP3463	
ET-LAN unit	AFP3790	
C.C.U.	AFP3462	
Data memory unit	AFP32091	16SX
	AFP32092	

☞ **Notes**

- **(*1): The number of I/O occupied points that units marked "16SE (0SE)" possess can be set to 0 using arbitrary allocation in the NPST-GR.**
- **(*2): I/O allocation for a MEWNET-TR transmitter master unit vary depending on the unit settings.**
- **The occupied I/O points are expressed in the following fashion for convenience.**



3.4 Table of I/O Occupied Points

Chapter 4

Installation and Wiring

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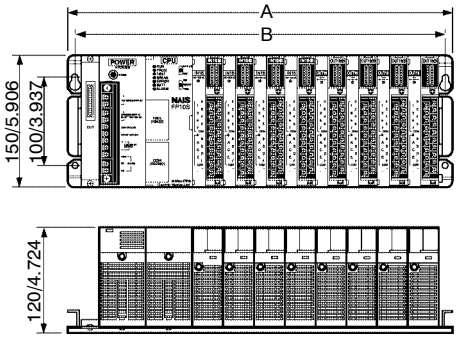
4.1 Installation

4.1.1 Installation Space and Environment

Dimensions

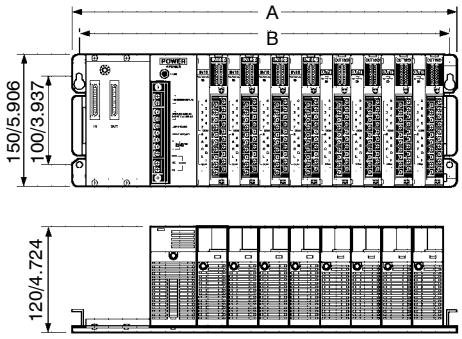
Master backplane



(unit: mm/in.)

Type	Overall length A (mm/in.):	Mounting hole pitch B (mm/in.):
3-slot type	260/10.236	245/9.646
5-slot type	330/12.992	315/12.402
8-slot type	435/17.126	420/16.535

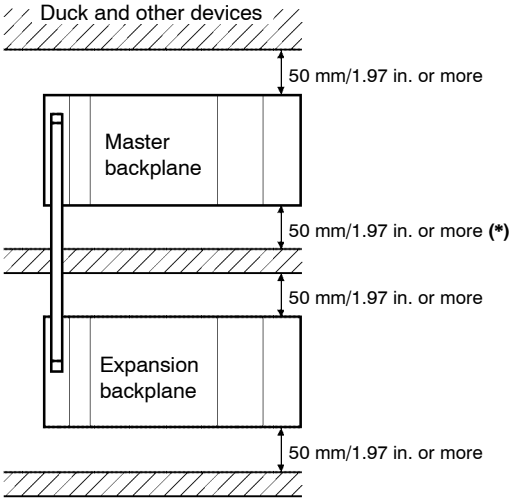
Expansion backplane



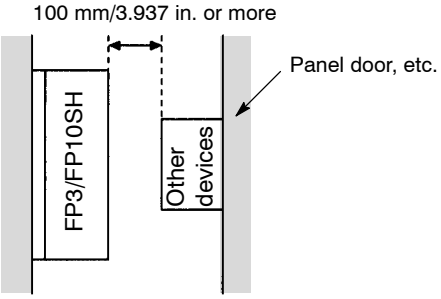
(unit: mm/in.)

Type	Overall length A (mm/in.):	Mounting hole pitch B (mm/in.):
3-slot type	260/10.236	245/9.646
5-slot type	330/12.992	315/12.402
8-slot type	435/17.126	420/16.535

Installation Space



(*): When using the MEWNET-P link unit: 80 mm/3.15 in. or more



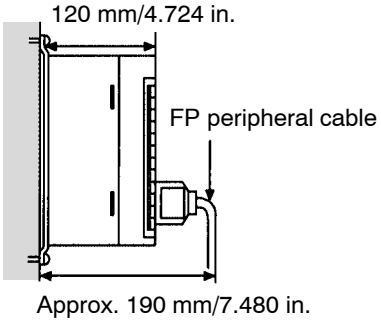
Leave at least 50 mm/1.97 in. of space between the peripheral ducts of the unit and other devices to allow heat radiation and unit replacement.

Leave some further space, as indicated below, around the lower section when using a link unit.
When using the MEWNET-P link unit: 80 mm/3.15 in. or more

When installing devices facing the FP3/FP10SH such as on the door of the panel, leave a space of at least 100 mm/3.94 in. between that device and the unit to avoid the effects of heat or radiated noise.

☞ next page

Although the depth of the unit is 120 mm/4.724 in., leave a space of at least 200 mm/7.87 in. from the mounting surface for programming tool connections and wiring.



Avoid installing the unit in the following locations:

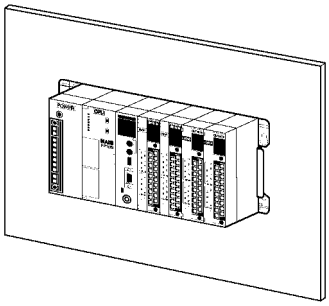
- Ambient temperatures outside the range of 0 to 55 °C/32 to 131 °F
- Ambient humidity outside the range of 30 to 85 % RH
- Sudden temperature changes causing condensation
- Inflammable or corrosive gases
- Excessive airborne dust or metal particles
- Benzine, paint thinner, alcohol, other organic solvents or strong alkaline solutions such as ammonia or caustic soda
- Excessive vibration or shock
- Direct sunlight
- Water in any from including spray or mist

Avoid noise interference from the following items:

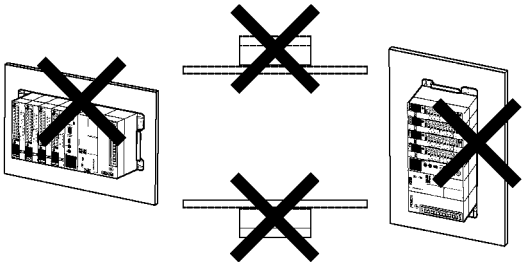
- Influence from power transmission lines, high voltage equipment, power cables, power equipment, radio transmitters, or any other equipment that generates high switching surges.

Measures regarding heat discharge

Install as shown below, for heat radiation.



Do not install the FP3/FP10SH unit as shown below.

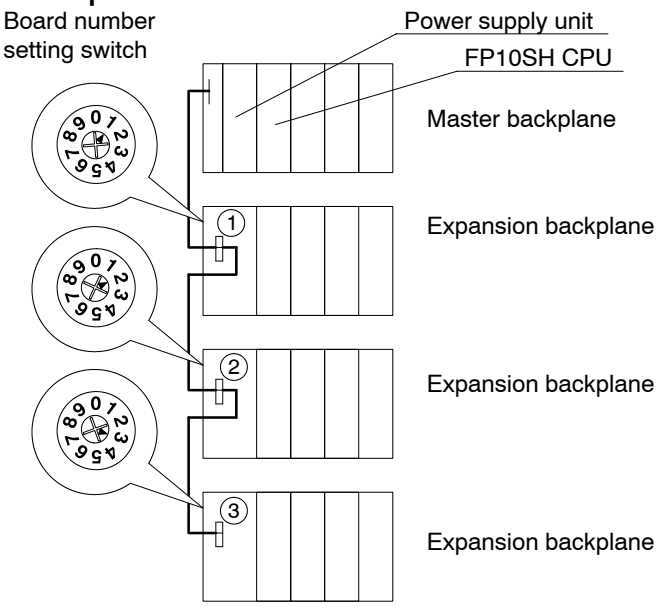


Do not install the unit above devices which generate heat such as heaters, transformers or large scale resistors.

4.1.1.1 Setting the Board Number

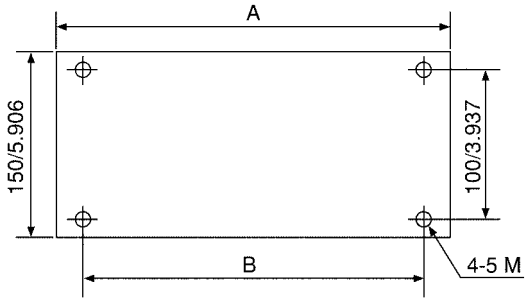
Set the board numbers in order starting with backplane nearest to the master backplane. Start with board number 1.

<Example> FP10SH



4.1.2 Mounting Method

Mounting hole dimensions



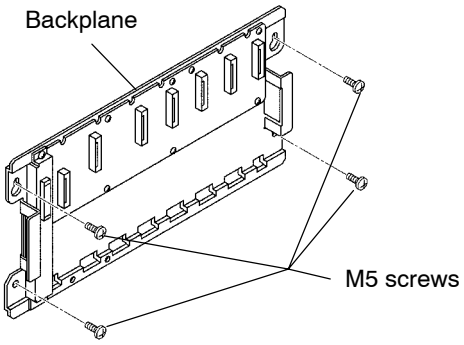
(unit: mm/in.)

Type	Number of slot	Order number	A (mm/in.)	B (mm/in.)
Master backplane	**3-slot**	AFP3505–F	260/10.236	245/9.646
	5-slot	AFP3501–F	330/12.992	315/12.402
	8-slot	AFP3502–F	435/17.126	420/16.535
Expansion backplane	**3-slot**	AFP3506–F	260/10.236	245/9.646
	5-slot	AFP3503–F	330/12.992	315/12.402
	8-slot	AFP3504–F	435/17.126	420/16.535

Mount the backplane using M5 screws according to the following procedure

Procedure:

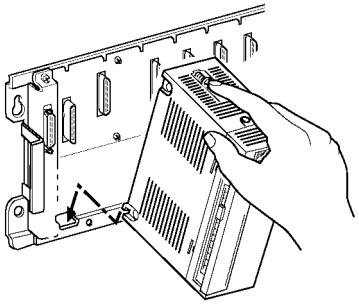
1. **Lightly secure the upper part of the backplane using the mounting holes.**
2. **Align the mounting holes for the lower part and secure.**
3. **Tighten the upper screws.**



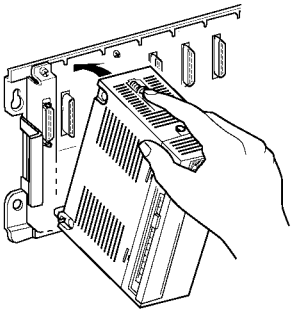
Install each unit using the supplied screws according to the following procedure.

Procedure:

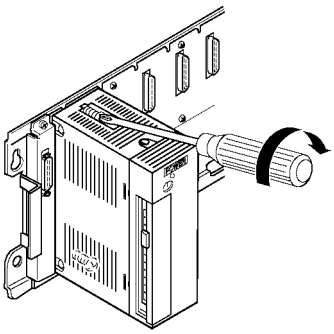
1. **Fit the two unit tabs into the unit holes on the backplane.**



2. **Push the unit in the direction of the arrow and install onto the backplane.**



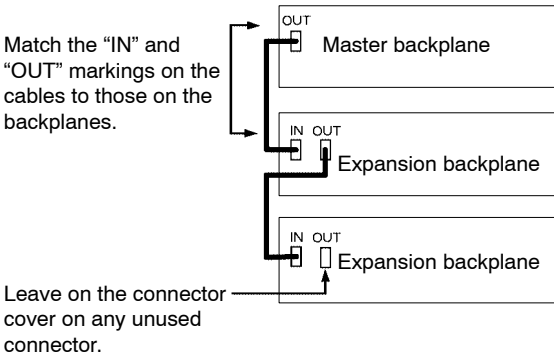
3. **After properly installing the unit to the backplane, secure the mounting screw at the top.**
   Secure the power supply unit and CPU with screws at both the top and bottom.



4.1.3 Connecting Expansion Cable

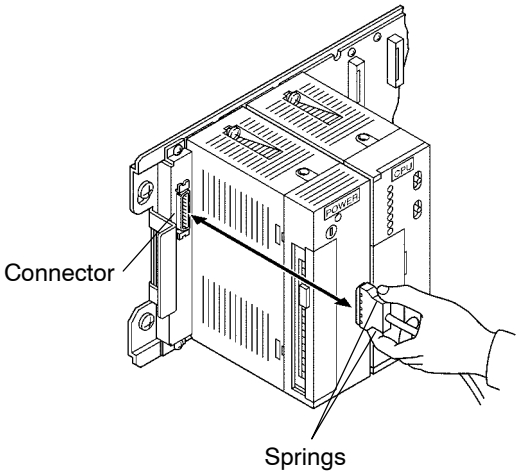
The expansion cables are directional and are equipped with a key to prevent erroneous insertion.

Connect so that the IN and OUT marks on the cable match the IN and OUT marks on the backplane.



Insert the expansion cables firmly until they click into place.

When removing the cable, hold down the springs on the side of the cable connector to release it from the locked condition and pull out the expasion cable.



☞ **Notes**

- **Leave on the dust proofing label on the upper surface of the unit until the wiring work is finished.**
- **Leave the connector covers on any unused slots to protect them from dust.**
  The same for the connector of expansion cable.

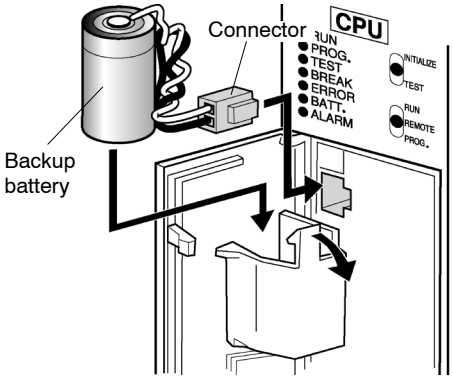
4.1.4 Connecting Backup Battery

The internal RAM of the CPU is backed up by the internal battery of the unit. Verify that it is properly connected before programming.

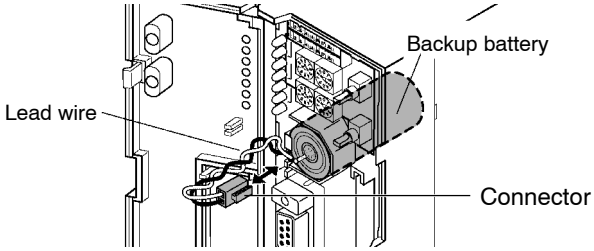
Procedure:

1. **Turn OFF power.**
2. **Open the cover of CPU.**
3. **Securely connect the backup battery connector.**
4. **When closing the cover, make sure it does not bite into the lead wire.**
5. **Turn ON power.**

FP3



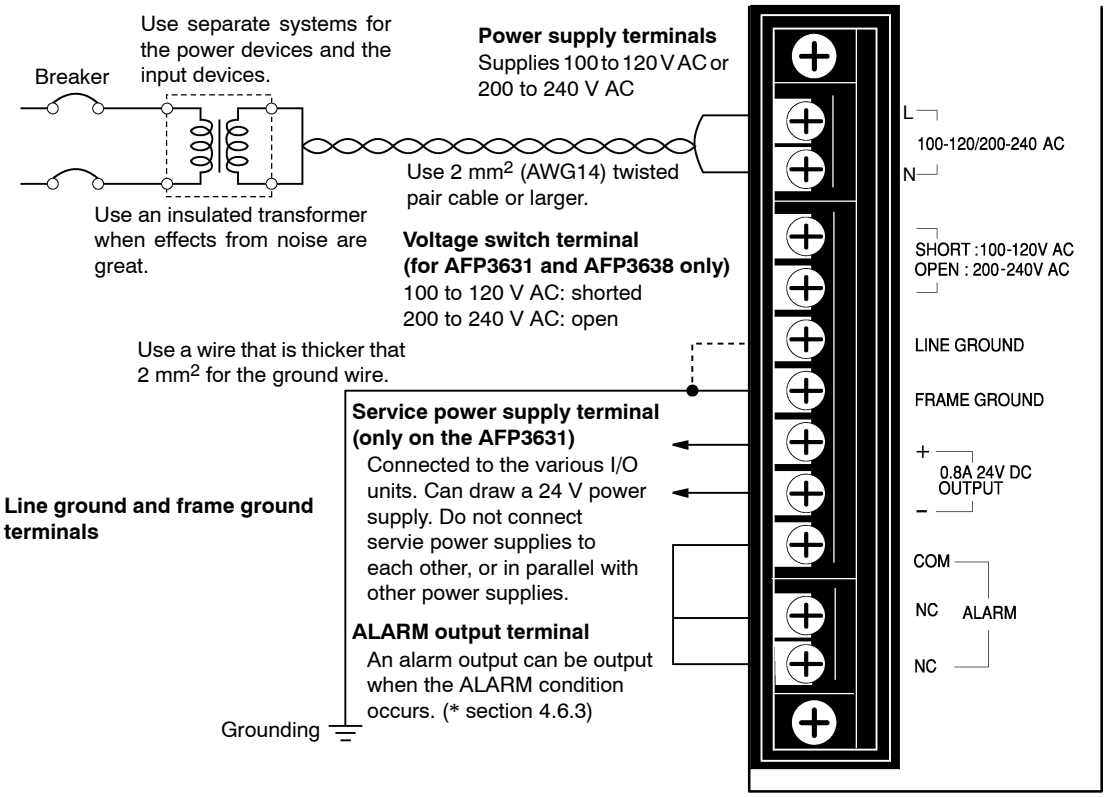
FP10SH



4.2 Power Supply Wiring

4.2.1 Wiring the Power Supply to the Power Supply Unit

Pin layout of power supply unit (AFP3631 is used for the example below.)



Power supply voltage

Verify that the power supply voltage is within allowable limits.

Type	Order number	Rated input voltage	Operating voltage range
AC type	**AFP3631, AFP3638**	100 to 120 V AC	85 to 132V AC
		200 to 240 V AC	170 to 264V AC
DC type	**AFP3634**	24 V DC	16.8 to 28.8 V DC

For the AFP3631 and AFP3638, switch between 100 V AC and 200 V AC with the voltage switch terminal.

Power supply wire

Use power supply wire that is thicker than 2 mm^2 to minimize the voltage drop.
Twist the electrical wire to minimize the effects of noise.

Voltage switch terminal

When using the power supply unit, AFP3631 and AFP3638:

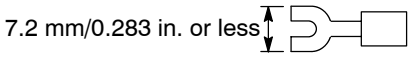
- When using 100 to 120 V AC, short the voltage switch terminal using the short circuiting bar included in the package.
- When using 200 to 240 V AC, check that the space between the terminals is open.

Pressure connection terminal

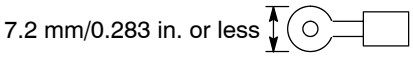
M3.5 screws are used for the terminals.

The following M3.5 pressure connection terminals are recommended for the wiring.

Fork type terminal

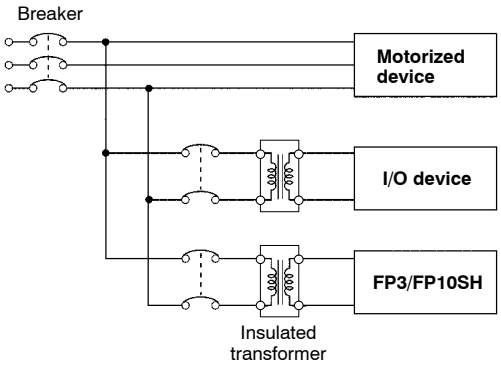


Round type terminal



Power supply system

Use separate wiring system for the FP3/FP10SH, input/output devices and motorized devices.



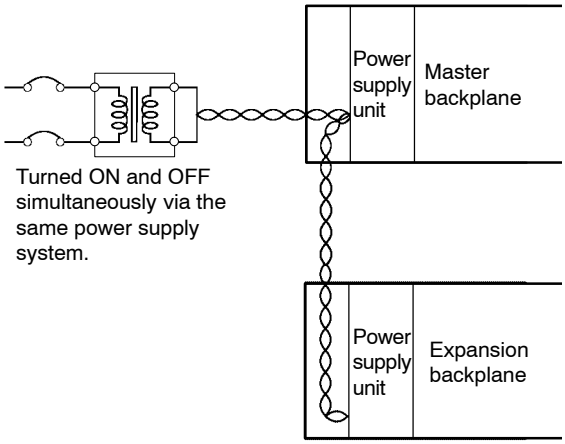
Eliminating effects from noise

Use a low noise power supply.

Excessive noise and line voltage fluctuations can result in FP3 or FP10SH CPU misoperation or in system shutdown. To prevent accidents caused by noise and line voltage fluctuations, be sure to employ countermeasures (such as use of an insulated transformer, etc.) when wiring the power supply lines.

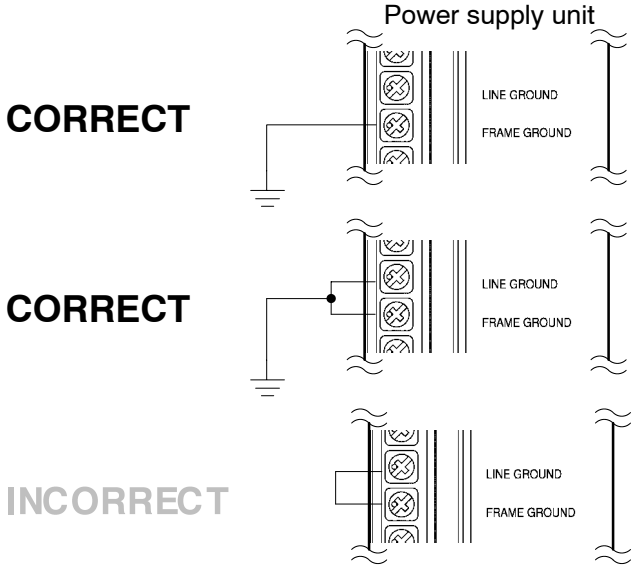
☞ **Note**

Use the same power supply system for the master and expansion backplanes so that they are turned ON and OFF simultaneously.

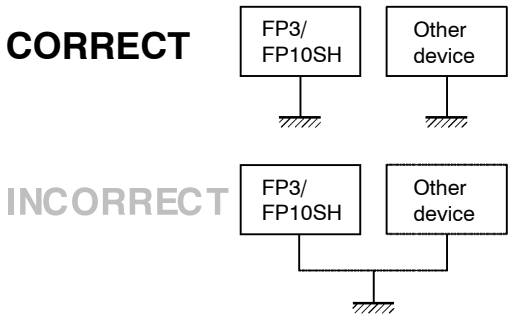


4.2.2 Grounding

The frame ground terminal (FRAME GROUND) is connected to the metallic part of the master backplane and is the terminal for connection to ground.
The line ground terminal (LINE GROUND) is the midpoint terminal for the internal noise filter.
When the effects from noise are large, ground as shown in the diagram below.
The line ground terminal (LINE GROUND) has an electric potential, so be sure to ground it to prevent electric shock when connecting it to the frame ground terminal (FRAME GROUND).



For grounding purposes, use ground wires with a **minimum of 2 mm^2** and the grounding connection should have a resistance of **less than 100** Ω.
The point of grounding should be as close to the FP3/FP10SH unit as possible.
The ground wire should be as short as possible.
If two devices share a single ground point, it may produce an adverse effect. Always use an exclusive ground for each device.



4.3 Wiring Input and Output

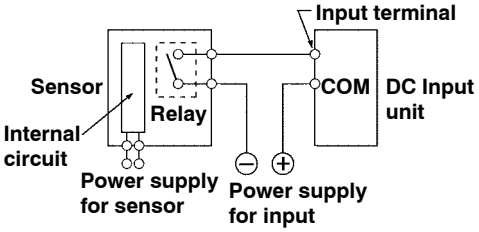
4.3.1 Input Wiring

There is a limit on the number of simultaneous ON points allowed on some units. Refer to the specifications page for each input unit (* sections 2.9 and 2.11). In particular, take care when using the units in locations with a high ambient temperature.

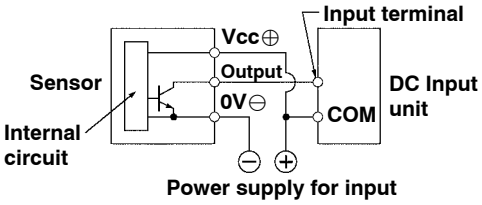
In this section you find some examples for wiring sensors, an AC input device, an LED-equipped reed switch, a two-wire type sensor and a LED-equipped limit switch.

4.3.1.1 Sensors

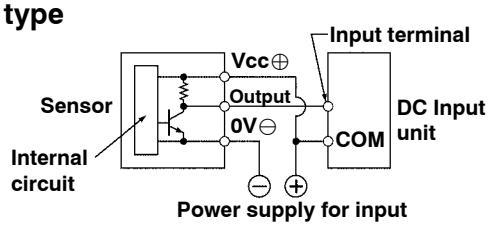
Relay output type



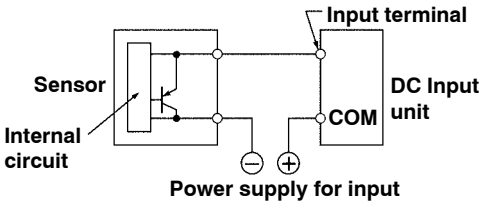
NPN open collector output type



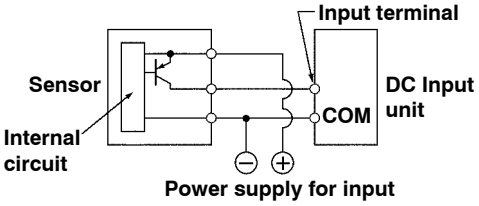
Voltage output (Universal output) type



Two-wire type (* section 4.3.1.4)

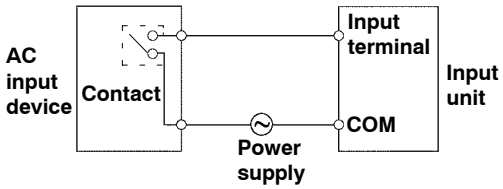


PNP open collector output type

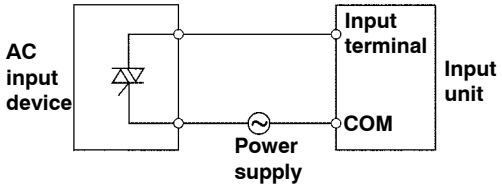


4.3.1.2 AC Input Devices

Contact output type

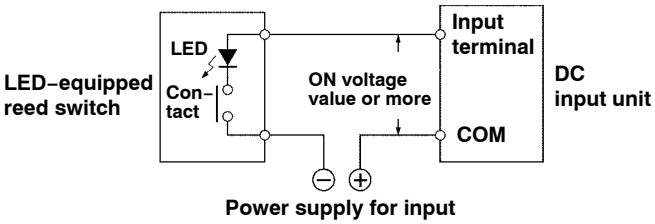


Non-contact output type



4.3.1.3 LED–Equipped Reed Switch

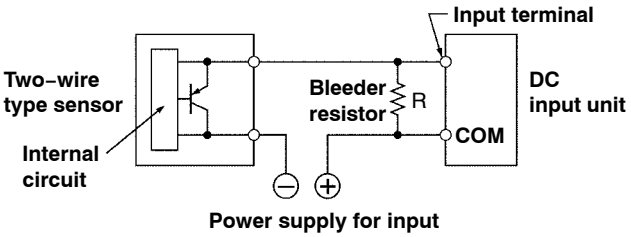
When a LED is connected to an input contact such as LED-equipped reed switch, make sure that the voltage value applied to the input terminal of FP3/FP10SH is greater than ON voltage value.
In particular, take care when connecting a number of switches in series.



4.3.1.4 Two–Wire Type Sensor

If the input of FP3/10SH is not turned OFF because of leakage current from the two–wire type sensor, the use of a bleeder resistor is recommended, as shown below.

Using 12 to 24 V DC type input unit
(OFF voltage: 2.5 V, Input impedance: 3 kΩ)



I: Sensor's leakage current (mA)
R: Bleeder resistor (kΩ)

☞ next page

The OFF voltage of the input is 2.5 V, therefore, select an R value so that the voltage between the COM terminal and the input terminal will be less than 2.5 V.
(The input impedance is 3 kΩ.)

The resistance R of the bleeder resistor is: $R \leqq \frac{7.5}{3 \times I - 2.5}$ (kΩ)

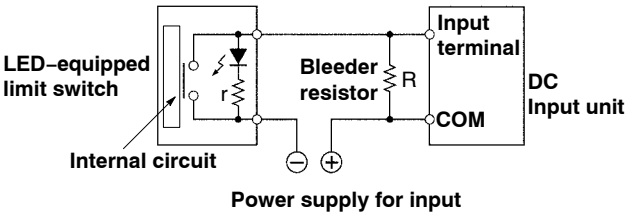
The wattage W of the resistor is: $W = \frac{(\text{Power supply voltage})^2}{R}$

In the actual selection, use a value that is 3 to 5 times the value of W.

4.3.1.5 LED–Equipped Limit Switch

If the input of the FP3/FP10SH is not turned OFF or if the LED of the limit switch is kept ON because of the leakage current, from the LED–equipped limit switch, the use of a bleeder resistor is recommended, as shown below.

Using 12 to 24 V DC type input unit
(OFF voltage: 2.5 V, Input impedance: 3 kΩ)



r: Internal resistor of limit switch (kΩ)
R: Bleeder resistor (kΩ)

The OFF voltage of the input is 2.5 V, therefore when the power supply voltage is 24 V, select R so that

The current will be greater than $I = \frac{24 - 2.5}{r}$

The resistance R of the bleeder resistor is: $R \leqq \frac{7.5}{3 \times I - 2.5}$ (kΩ)

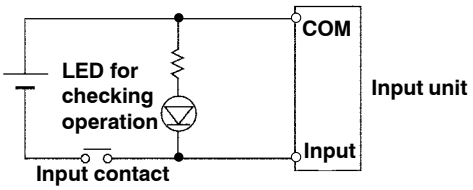
The wattage W of the resistor is: $W = \frac{(\text{Power supply voltage})^2}{R}$

In the actual selection, use a value that is 3 to 5 times the value of W.

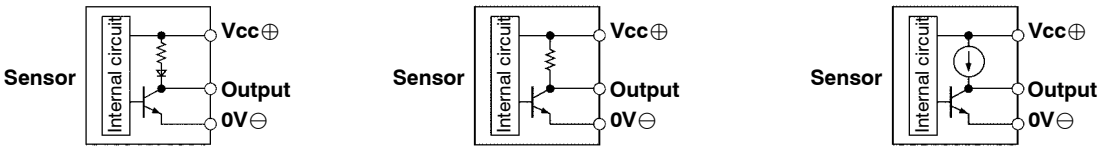
4.3.1.6 Wiring 64−point Type Input Unit

If the dip switch position (* section 2.9.3.4) on the rear side of the 64−point type input unit is set to ON position in the following situations, the current will wrap around as a result of the switching circuit, causing erroneous operation. In these situations, set the dip switch on the rear side of the 64−point type input unit to OFF position or insert a diode as shown below in example diagram.

To add an LED for checking operation in parallel with the input contact



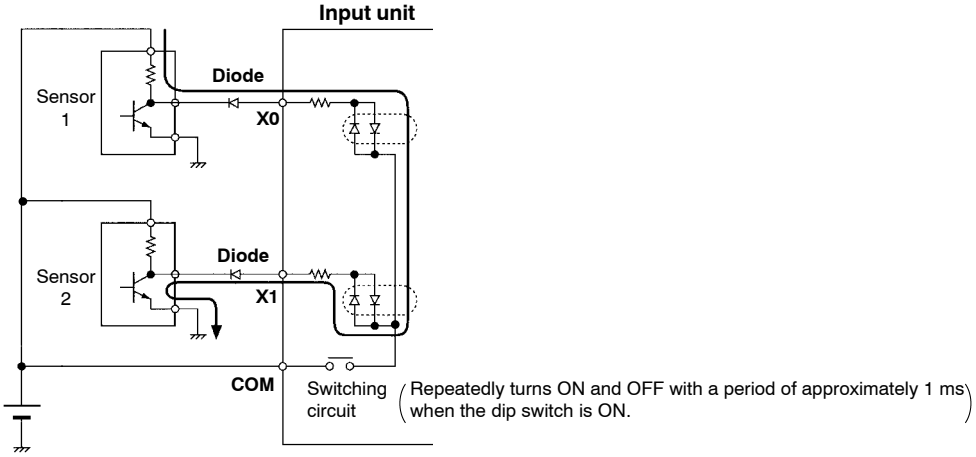
When using a non-open collector transistor output type for the sensor as shown in the diagram below



Example:

Wrap around when using a photoelectric sensor

In the diagram below, when the switching circuit goes OFF when sensor 1 is OFF and sensor 2 is ON, the current will flow as if on a thick wire, so that X0 and X1 will both go ON even though sensor 1 is OFF.



4.3.2 Output Wiring

There is a limit on the number of simultaneous ON points or load currents allowed on some units. Refer to the specifications page for each unit (* sections 2.10 and 2.11). In particular, take care when using the units in locations with high ambient temperatures.

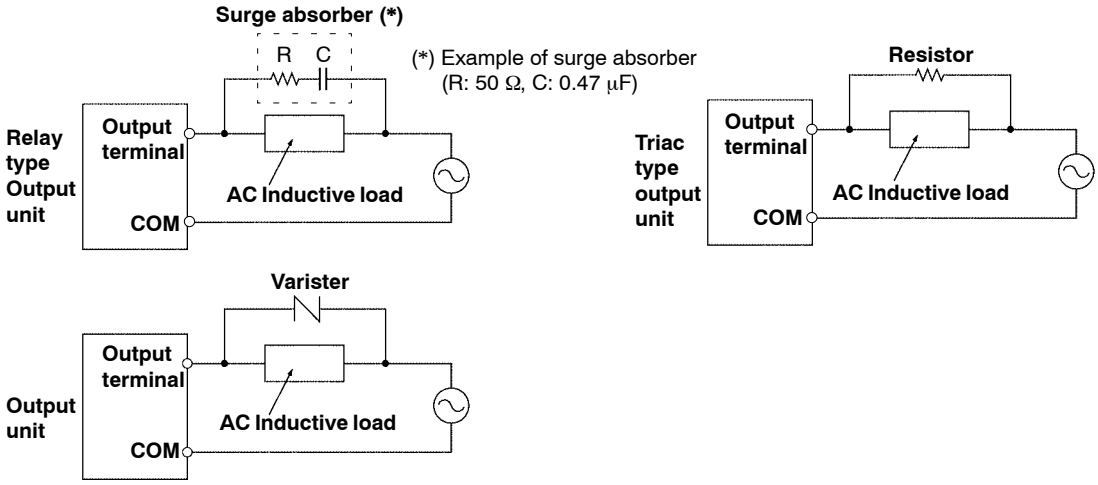
Use a protective circuit when connecting inductive load and capacitive load (* section 4.3.2.1 and 4.3.2.2).

Some output units have a limit on currents per the common. Use within that range.

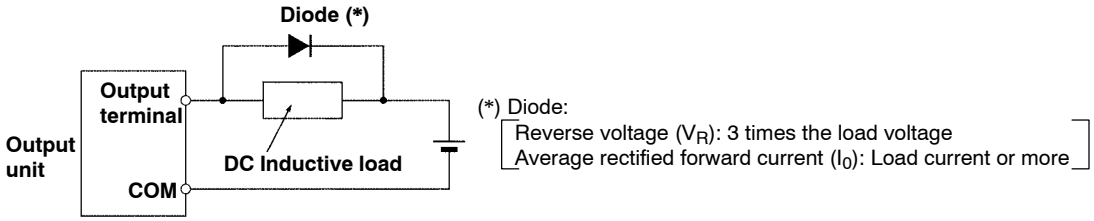
4.3.2.1 Protective Circuit for Inductive Loads

With an inductive load, a protective circuit should be connected in parallel with the load. When switching DC inductive loads with relay output type output unit, be sure to connect a diode across the ends of the load.

When using an AC inductive load

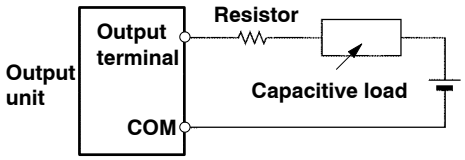


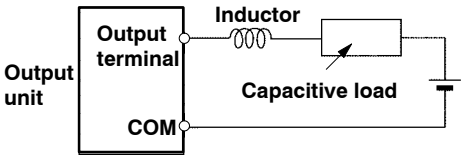
When using a DC inductive load



4.3.2.2 Protective Circuit for Capacitive Loads

When connecting the loads with large in−rush currents, to minimize their effect, connect a protection circuit as shown below.



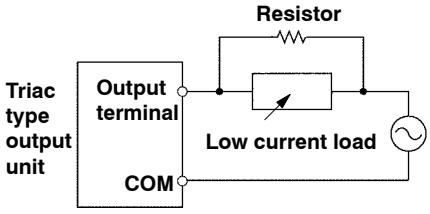


4.3.2.3 Precautions for Overload

The objective for output units with fuses is to prevent a burn out when an output short circuits, etc. Since it is not possible to protect each element against overload even for output units with fuses, it is recommended to connect an external fuse for each point. However, there are cases where it is not possible to protect the elements of the output unit when a short circuit occurs.

4.3.2.4 Precautions for Leakage Current

When there is a low current load with the triac type output unit, the load may not go OFF because of the leakage current. If this type of trouble should arise, connect a resistor in parallel with the load, as shown below.



4.3.3 Cautions Regarding Input and Output Units

Wiring

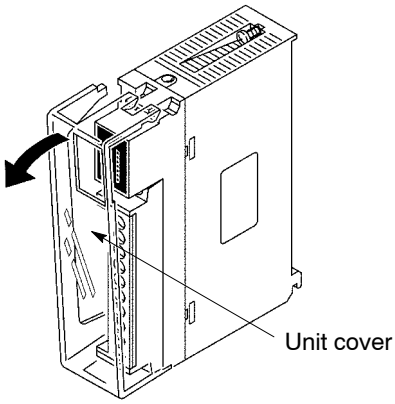
Arrange the wiring so that the input and output wiring are separated, and so that the input and output wiring is separated from the motorized wiring, as so much as possible. Do not route them through the same duct or wrap them up together.

Separate the wires of input/output from the motorized and high voltage wires by at least 100 mm/3.937 in.

Unit cover

Attach and remove the cover of the input and output unit as shown below.

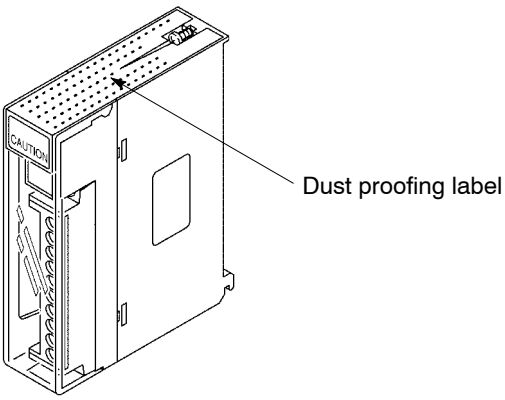
The unit cover cannot be attached when using the connector for wire−pressed terminal cable with hood cover in the connector type unit.



Dust proofing label

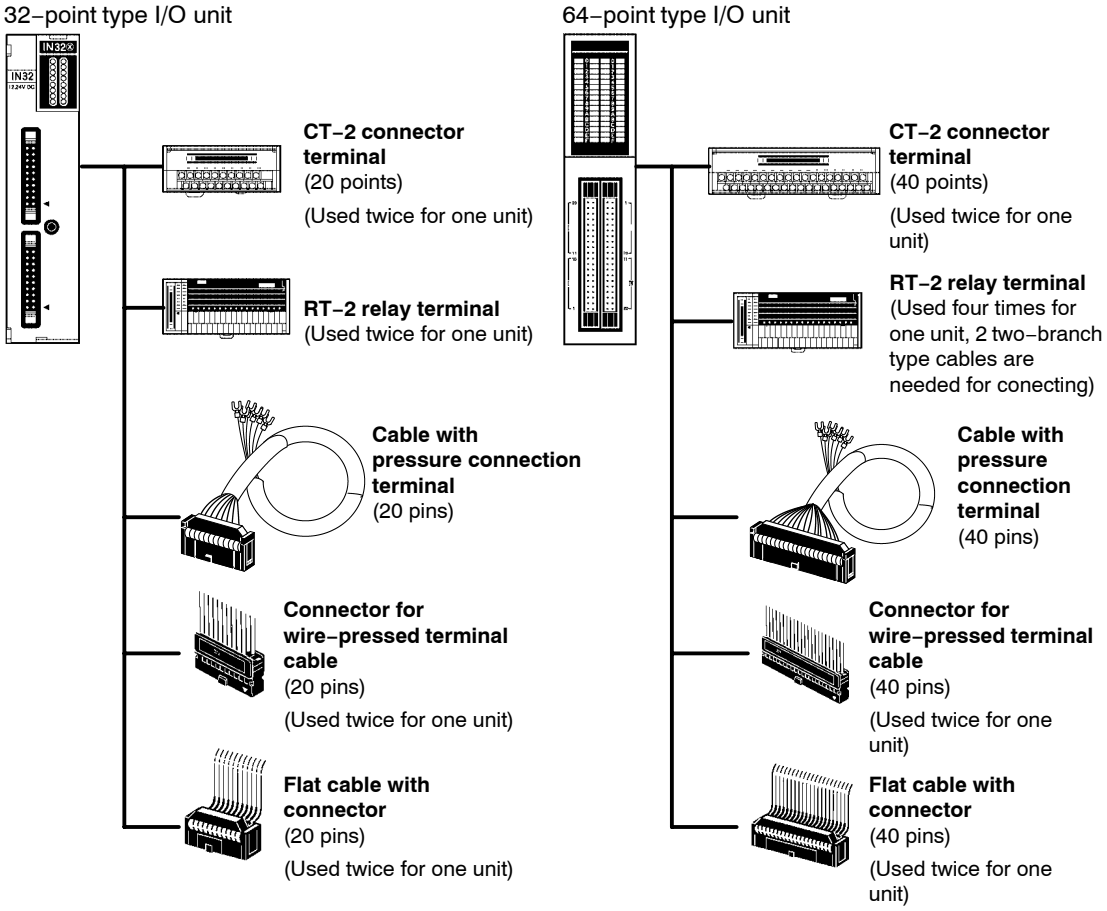
Do not remove the dust proofing label that is attached to the upper portion of the unit until the installation and wiring are finished.

Be sure to remove the dust proofing label prior to operation to allow heat radiation.



4.4 Wiring the Connector Type I/O Units

4.4.1 Wiring the Connector Type Units



Wiring method
When using connector and relay terminals (* section 4.4.2):

- Can be connected using exclusive cables, eliminating the bother of wiring
- With the RT−2 relay terminal, you can control up to 2 A, and maintenance such as relay replacement is easy
- Economical for input wiring and transistor output wiring by the CT−2 connector terminal

☞ next page

When using cable with pressure connection terminal (* section 4.4.3)

- The connector converted to a pressure connection terminal using the connector terminal cable.
- The correspondence between the I/O numbers and pressure connection terminal pin numbers are the same as for connector terminals. (* section 4.4.2)

When using connector for wire–pressed terminal cable (* section 4.4.4)

- You can directly connect wires from 0.2 to 0.3 mm^2.
- Eliminates the bother of wiring connections because the wires can be connected without removing the covers from the wires.
- Can correct wiring mistakes smoothly.
- A tool exclusively designed for this purpose is necessary.

When using flat cable (* section 4.4.5)

- There is a cable with a connector on only one end.
- When using a commercially available flat cable, be sure to use a suitable connector.

☞ next page

Type of unit				32-point type Input unit	32-point type Output unit	64-point type Input unit	64-point type Output unit	64-point type I/O mixed unit	
				AFP33024–F AFP33014–F	AFP33484–F AFP33584–F (*Note 1)	AFP33027–F AFP33017–F AFP33028–F AFP33068–F	AFP33487–F AFP33587–F (*Note 1)	AFP33428–F AFP33528–F (*Note 1)	
								Input	Output
Number of connector pins				20		40		40	
Using terminal	CT–2 connector terminal	DIN rail mounting type		AYC1120		AYC1140		AYC1140	
		Direct mounting type		AVC2120		AYC2140		AYC2140	
		Exclusive cable	1 m/ 3.281ft	AYT51203		AYT51403		AYT51403	
			2 m/ 6.562ft	AYT51205		AYT51405		AYT51405	
	RT–2 relay terminal	DIN rail mounting type		–	AY232502	–	AY232502	–	AY232502
		Direct mounting type		–	AY232522	–	AY232522	–	AY232522
		Exclusive cable	1 m/ 3.281ft	–	AY15133	–	AY15633	–	AY15633
			2 m/ 6.562ft	–	AY15135	–	AY15635	–	AY15635
Using cable with pressure connection terminal	1 m/3.281ft			AYT58203		AYT58403		AYT58403	
	2 m/6.562ft			AYT58205		AYT58405		AYT58405	
Using connector for wire–pressed terminal cable		Housing		AXW1204A (2 pieces)		AXW1404A (2 pieces)		AXW1404A (2 pieces)	
		Contact		AXW7221 (2 pieces) (5 pins/line) (*Note 2)		AXW7221 (4 pieces) (5 pins/line) (*Note 2)			
		Semi-cover		AXW62001A (2 pieces)		AXW64001A (2 pieces)		AXW64001A (2 pieces)	
		Pressure connector tool		AXY52000					
Using flat cable	Flat cable with a connector on one end		1 m/ 3.281ft	–	–	AFB8541		AFB8541	
			2 m/ 6.562ft	–	–	AFB8542		AFB8542	
	Connector only			AXM120415		AXM140415		AXM140415	

☞ Notes

- **(*1): The RT–2 relay terminal cannot be used in the PNP open collector output type units AFP33584–F, AFP33587–F, and AFP33528–F.**
- **(*2): When ordering, please contact your dealer regarding the minimum quantity.**

4.4.2 Connecting the Terminals

4.4.2.1 CT−2 Connector Terminal

For 32−point type I/O units, use a 20−pin type CT−2 connector terminal. For 64−point type I/O units, use a 40−pin type CT−2 connector terminal.

For connecting the terminal to the terminal block, use M3−sized pressure connection terminals.

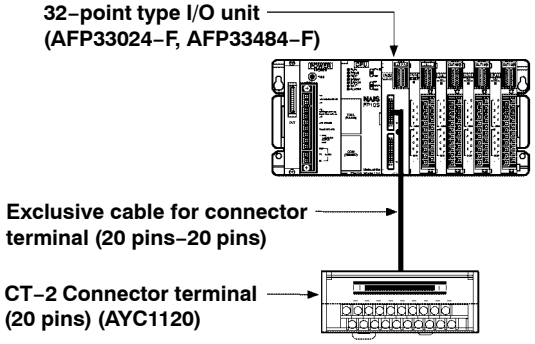
If using the CT−2 connector terminal for the input, connect between the COM terminals.

If using the CT−2 connector terminal for the output, 24 V DC should be supplied between (+) and (−) terminals. Power is supplied to drive the internal circuit of the output unit. Connect between each the (+) terminals and between each the (−) terminals.

☞ next page

The correspondence between the terminal numbers of CT−2 connector terminal and the I/O numbers of the I/O unit is shown in the table below.

Correspondence−CT−2 connector terminal and 32−point type I/O unit

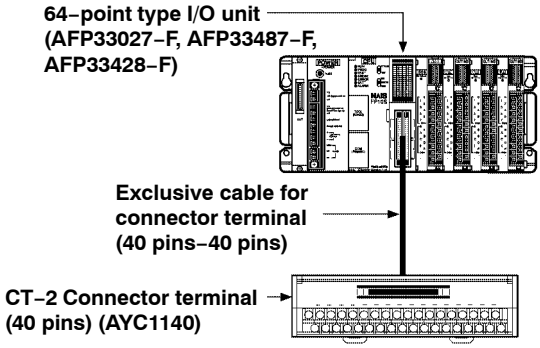


Terminal number	Unit symbol	Input number	Output number		Terminal number	Unit symbol	Input number	Output number
A1	I1	X0	Y0		**B1**	II1	X8	Y8
A2	I2	X1	Y1		**B2**	II2	X9	Y9
A3	I3	X2	Y2		**B3**	II3	XA	YA
A4	I4	X3	Y3		**B4**	II4	XB	YB
A5	I5	X4	Y4		**B5**	II5	XC	YC
A6	I6	X5	Y5		**B6**	II6	XD	YD
A7	I7	X6	Y6		**B7**	II7	XE	YE
A8	I8	X7	Y7		**B8**	II8	XF	YF
A9	I9	COM	−		**B9**	II9	COM	−
A10	I10	N.C.	+		**B10**	II10	N.C.	+

☞ **Note**

The above table shows the I/O numbers assuming connection to the connector (I, II) on the upper side of the 32−point type I/O unit. If connection has been made to the connector (III, IV) on the lower side, the I/O number allocations in the above table should be read as shown below, e.g.:
A1 . . . . Input X10, Output Y10
B1 . . . . Input X18, Output Y18

Correspondence–CT–2 connector terminal and 64–point type I/O unit



Terminal number	Input number	Output number	Terminal number	Input number	Output number
A1	X0	Y0	**B1**	X8	Y8
A2	X1	Y1	**B2**	X9	Y9
A3	X2	Y2	**B3**	XA	YA
A4	X3	Y3	**B4**	XB	YB
A5	X4	Y4	**B5**	XC	YC
A6	X5	Y5	**B6**	XD	YD
A7	X6	Y6	**B7**	XE	YE
A8	X7	Y7	**B8**	XF	YF
A9	COM	–	**B9**	COM	–
A10	N.C.	+	**B10**	N.C.	+
A11	X10	Y10	**B11**	X18	Y18
A12	X11	Y11	**B12**	X19	Y19
A13	X12	Y12	**B13**	X1A	Y1A
A14	X13	Y13	**B14**	X1B	Y1B
A15	X14	Y14	**B15**	X1C	Y1C
A16	X15	Y15	**B16**	X1D	Y1D
A17	X16	Y16	**B17**	X1E	Y1E
A18	X17	Y17	**B18**	X1F	Y1F
A19	COM	–	**B19**	COM	–
A20	N.C.	+	**B20**	N.C.	+

☞ Note

The above table shows the I/O numbers assuming connection to the connector (CN1) of the 64–point type I/O unit. If connection has been made to the connector (CN2), the I/O number allocations in the above table should be read as shown below, e.g.:
A1 . . . . Input X20, Output Y20
A11 . . . Input X30, Output Y30

4.4.2.2 RT−2 Relay Terminal

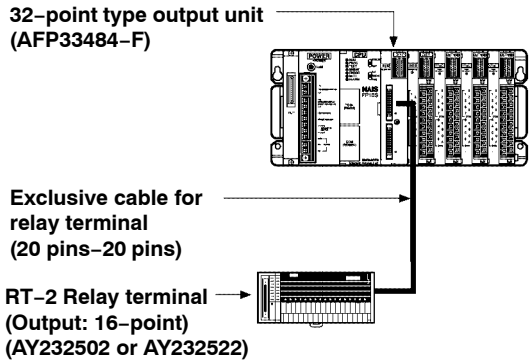
For 32−point type output unit, you can connect two sets of the RT−2 relay terminals with 16 outputs.

For 64−point type output unit, you can connect four sets of the RT−2 relay terminals with 16 outputs by using two−branch type cable.

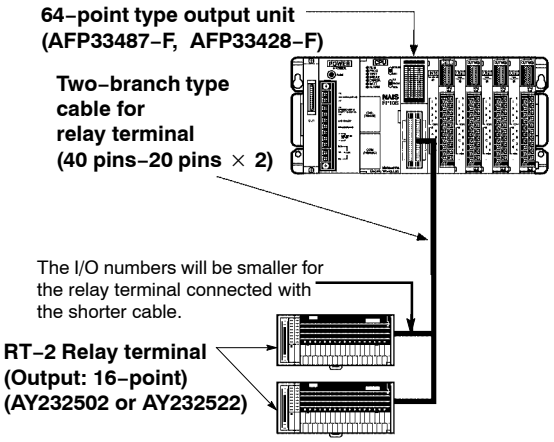
For connecting the terminal to the terminal block, use M3−sized pressure connection terminals.

24 V DC should be supplied between the (+) and (−) terminals of the relay terminal. This supplies the power to drive the relays of the terminal itself and the power to drive the internal circuit of the output unit.

32−point type output unit to RT−2 relay terminal



64−point type output unit to RT−2 relay terminal



☞ **Note**

When using the relay RT−2 terminal, the I/O power supply supplied to the units and the power supply supplied to the RT−2 relay terminals are the same power supply.

Correspondence–RT–2 relay terminal and I/O unit

The correspondence between the terminal numbers of RT–2 relay terminal and the I/O numbers of the I/O unit is shown in the table below. The output terminals have four points per common.

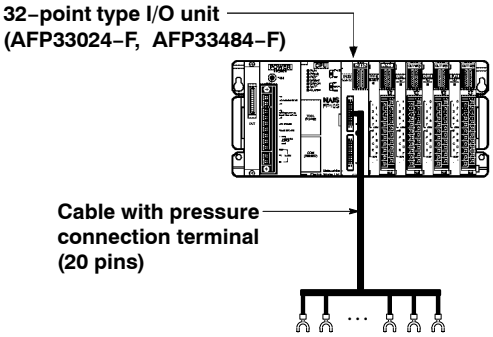
Terminal number	Output number		Terminal number	Output number
0+	Y0		**8+**	Y8
1+	Y1		**9+**	Y9
2+	Y2		**A+**	YA
3+	Y3		**B+**	YB
COM–	Common terminal for Y0 to Y3		**COM–**	Common terminal for Y8 to YB
4+	Y4		**C+**	YC
5+	Y5		**D+**	YD
6+	Y6		**E+**	YE
7+	Y7		**F+**	YF
COM–	Common terminal for Y4 to Y7		**COM–**	Common terminal for YC to YF

4.4.3 Connecting the Cable With Pressure Connection Terminal

For 32−point type I/O units, use a 20−pin type cable with pressure connection terminal. For 64−point type I/O units, use a 40−pin type cable with pressure connection terminal. The M3.5−sized pressure connection terminals are used for the cable with pressure connection terminal.

The correspondence between the terminal number of cable with pressure connection terminals and the I/O numbers of the I/O unit is shown in the table below.

Correspondence−Cable with pressure connection terminal and 32−point type I/O unit

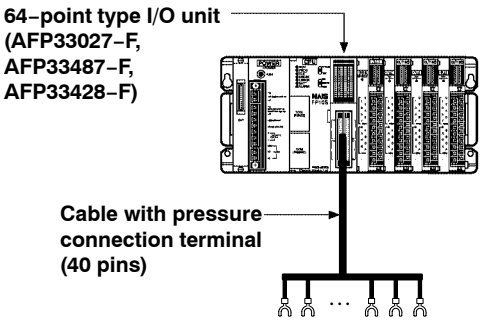


Terminal number	Unit symbol	Input number	Output number		Terminal number	Unit symbol	Input number	Output number
A1	I1	X0	Y0		**B1**	II1	X8	Y8
A2	I2	X1	Y1		**B2**	II2	X9	Y9
A3	I3	X2	Y2		**B3**	II3	XA	YA
A4	I4	X3	Y3		**B4**	II4	XB	YB
A5	I5	X4	Y4		**B5**	II5	XC	YC
A6	I6	X5	Y5		**B6**	II6	XD	YD
A7	I7	X6	Y6		**B7**	II7	XE	YE
A8	I8	X7	Y7		**B8**	II8	XF	YF
A9	I9	COM	−		**B9**	II9	COM	−
A10	I10	N.C.	+		**B10**	II10	N.C.	+

☞ **Note**

The above table shows the I/O numbers assuming connection to the connector (I, II) on the upper side of the 32−point type I/O unit. If connection has been made to the connector (III, IV) on the lower side, the I/O number allocations in the above table should be read as shown below, e.g.:
A1 . . . . Input X10, Output Y10
B1 . . . . Input X18, Output Y18

Correspondence–Cable with pressure connection terminal and 64–point type I/O unit



Terminal number	Input number	Output number		Terminal number	Input number	Output number
A1	X0	Y0		**B1**	X8	Y8
A2	X1	Y1		**B2**	X9	Y9
A3	X2	Y2		**B3**	XA	YA
A4	X3	Y3		**B4**	XB	YB
A5	X4	Y4		**B5**	XC	YC
A6	X5	Y5		**B6**	XD	YD
A7	X6	Y6		**B7**	XE	YE
A8	X7	Y7		**B8**	XF	YF
A9	COM	–		**B9**	COM	–
A10	N.C.	+		**B10**	N.C.	+
A11	X10	Y10		**B11**	X18	Y18
A12	X11	Y11		**B12**	X19	Y19
A13	X12	Y12		**B13**	X1A	Y1A
A14	X13	Y13		**B14**	X1B	Y1B
A15	X14	Y14		**B15**	X1C	Y1C
A16	X15	Y15		**B16**	X1D	Y1D
A17	X16	Y16		**B17**	X1E	Y1E
A18	X17	Y17		**B18**	X1F	Y1F
A19	COM	–		**B19**	COM	–
A20	N.C.	+		**B20**	N.C.	+

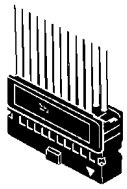
☞ **Note**

The above table shows the I/O numbers assuming connection to the connector (CN1) of the 64–point type I/O unit. If connection has been made to the connector (CN2), the I/O number allocations in the above table should be read as shown below, e.g.:
A1 . . . . Input X20, Output Y20
A11 . . . Input X30, Output Y30

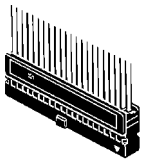
4.4.4 Connecting with Connector for Wire−pressed Terminal Cable

This is a connector that allows lose wires to be connected without removing the wire's insulation.

The pressure connection tool (AXY52000) is required to connect the loose wires.



Connector for wire−pressed terminal cable (20 pins)



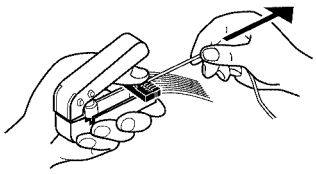
Connector for wire−pressed terminal cable (40 pins)

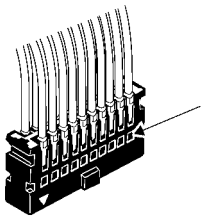
Suitable wires (twisted wire)

Size	Cross section area	Insulation thickness	Rated current
AWG22	0.3 mm^2	dia. 1.5 to dia. 1.1	3 A
AWG24	0.2 mm^2		

Contact puller pin for rewiring

If there is a wiring mistake or the wire is incorrectly pressure−connected, the contact puller pin provided with the fitting can be used to remove the contact.





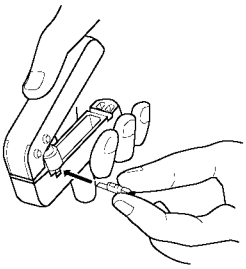
Press the housing against the pressure connection tool so that the contact puller pin comes in contact with this section.

Assembly of connector for wire−pressed terminal cable

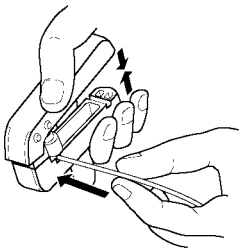
The wire end can be directly press−fitted without removing the wire‘s insulation, saving labor.

Procedure:

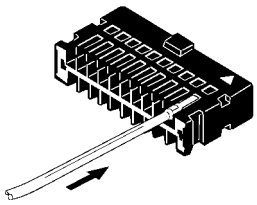
1. **Bend the contact back from the carrier, and set it in the pressure connection tool.**



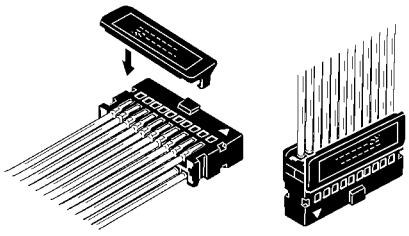
2. **Insert the wire without removing its insulation until it stops, and lightly grip the tool.**



3. **After press−fitting the wire, insert it into the housing.**



4. **When all wires has been inserted, fit the semi−cover into place.**



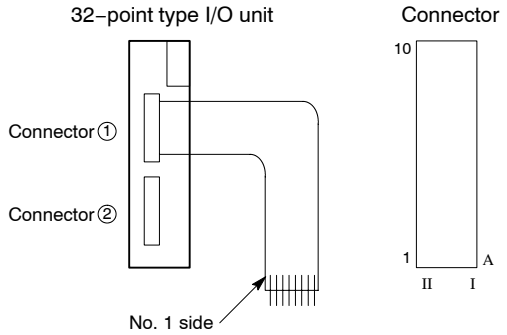
4.4.5 Connecting with Flat Cable Connector

Suitable wires (twisted wire)

Size	Pitch	Rated current
AWG28 (7 pcs./dia. 0.127)	1.27 mm	1 A

When connecting with a flat cable connector, the correspondence between the cable numbers and I/O number is shown in the table below.

Flat cable connection diagram for the 32–point type I/O unit



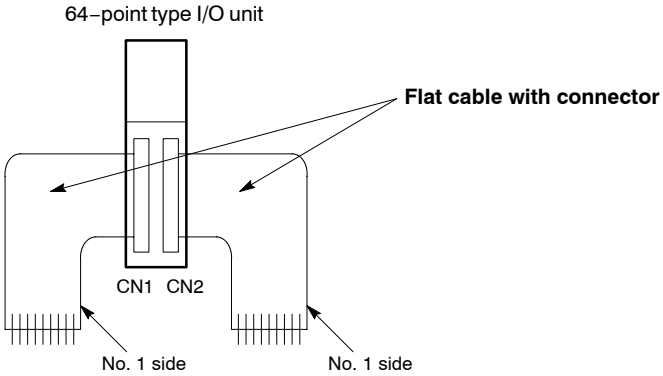
Correspondence–flat cable number and I/O number (32 points)

Cable number	Unit symbol	Input number	Output number		Cable number	Unit symbol	Input number	Output number
1	I1	X0	Y0		**11**	I6	X5	Y5
2	II1	X8	Y8		**12**	II6	XD	YD
3	I2	X1	Y1		**13**	I7	X6	Y6
4	II2	X9	Y9		**14**	II7	XE	YE
5	I3	X2	Y2		**15**	I8	X7	Y7
6	II3	XA	YA		**16**	II8	XF	YF
7	I4	X3	Y3		**17**	I9	COM	–
8	II4	XB	YB		**18**	II9	COM	–
9	I5	X4	Y4		**19**	I10	N.C.	+
10	II5	XC	YC		**20**	II10	N.C.	+

☞ **Note**

The above table shows the I/O numbers assuming connection to the connector ① on the upper side of the 32–point type I/O unit. If connection has been mode to the connector ② on the lower side, the I/O number allocation in the above table should be read as shown below, e.g.:
Cable No.1 . . . . Input X10, Output Y10
Cable No.2 . . . . Input X18, Output Y18

Flat cable connection diagram for the 64–point type I/O unit



Correspondence–flat cable number and I/O number (64 points)

Cable number	Input number	Output number		Cable number	Input number	Output number
1	X0	Y0		**21**	X10	Y10
2	X8	Y8		**22**	X18	Y18
3	X1	Y1		**23**	X11	Y11
4	X9	Y9		**24**	X19	Y19
5	X2	Y2		**25**	X12	Y12
6	XA	YA		**26**	X1A	Y1A
7	X3	Y3		**27**	X13	Y13
8	XB	YB		**28**	X1B	Y1B
9	X4	Y4		**29**	X14	Y14
10	XC	YC		**30**	X1C	Y1C
11	X5	Y5		**31**	X15	Y15
12	XD	YD		**32**	X1D	Y1D
13	X6	Y6		**33**	X16	Y16
14	XE	YE		**34**	X1E	Y1E
15	X7	Y7		**35**	X17	Y17
16	XF	YF		**36**	X1F	Y1F
17	COM	–		**37**	COM	–
18	COM	–		**38**	COM	–
19	N.C.	+		**39**	N.C.	+
20	N.C.	+		**40**	N.C.	+

☞ Note

The above table shows the I/O numbers assuming connection to the connector (CN1) on the left side. If connection has been made to the connector (CN2) on the right side, the I/O number allocations in the above table should be read as shown below, e.g.:

Cable No.1 . . . . Input X20, Output Y20

4.5 Wiring the Terminal Type I/O Units

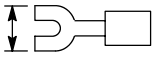
4.5.1 Wiring the Terminal Type Units

Pressure connection terminals

M3.5 terminal screws are used for the terminals of input and output units. The following pressure connection terminals are recommended for the wiring to the terminals.

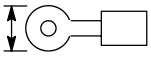
Fork type terminal

7.2 mm/0.283 in. or less



Round type terminal

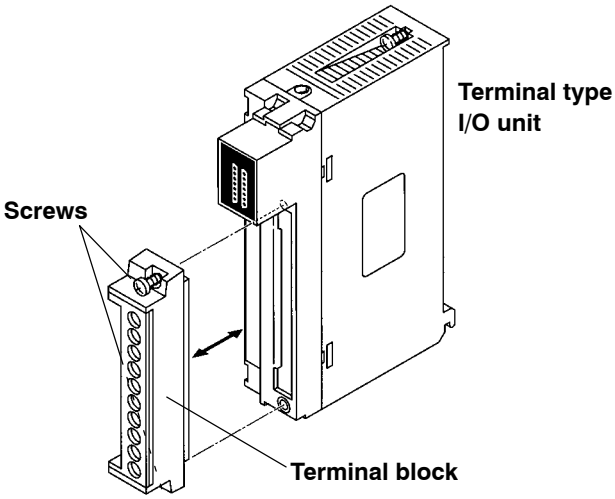
7.2 mm/0.283 in. or less



Wiring to terminal block

If the screws at both ends of the terminal block of the terminal type input and output units are loosened, the terminal block can be pulled out while the wiring is still connected.

Do not forget to tighten these screws after the wiring is completed.



4.6 Safety Measures

4.6.1 Safety Instructions

4.6.1.1 Precautions Regarding System Design

In certain applications, malfunction may occur for the following reasons:

- Power ON timing differences between the FP3/FP10SH system and I/O or motorized devices
- An operation time lag when a momentary power failure occurs
- Abnormality in the FP3/FP10SH, power supply circuit, or other devices

In order to prevent a malfunction resulting in system shutdown choose the adequates safety measures listed in the following:

4.6.1.2 Interlock Circuit

When a motor clockwise/counter-clockwise operation is controlled, provide an interlock circuit that prevents clockwise and counter-clockwise signals from inputting into the motor at the same time.

4.6.1.3 Emergency Stop Circuit

Add an emergency stop circuit to controlled devices in order to prevent a system shutdown or an irreparable accident when malfunction occurs.

4.6.1.4 Start Up Sequence

The FP3/FP10SH should be operated after all of the outside devices are energized. To keep this sequence, the following measures are recommended:

- Set the mode selector from PROG. mode to RUN mode after power is supplied to all of the outside devices.
- Program the FP3/FP10SH so as to disregard the inputs and outputs until the outside devices are energized.

4.6.1.5 Alarm Function

When an alarm occurs, the FP3/FP10SH turns OFF the output and stops operation. Even while in this condition, take the appropriate safety precautions outside of the FP3/FP10SH to ensure no malfunction or damage is transmitted to anywhere else in the system.

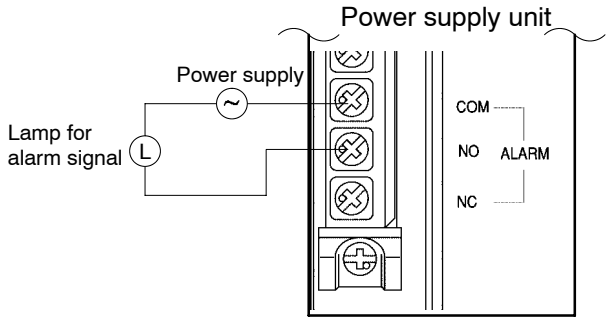
4.6.2 Momentary Power Failures

If a momentary power failure occurs, the resulting operations will differ depending on the duration of the power failure.

- Less than 10 ms: Operation continues.
- Between 10 ms and 20 ms: Depending on the conditions, the operation may continue or may stop.
- More than 20 ms: The unit resets and the output turns OFF. When the power returns, operation starts from its initial conditions.

4.6.3 Alarm Output

The alarm output goes ON when the watchdog timer (* section 4.6.3.1) is activated by a program error (eg., infinite loop) or an error in the hardware itself.
The alarm output terminal has two relay contacts, N.O. (normally open) and N.C. (normally closed) on the power supply unit, which can be used as external alarm signals.



☞ **Note**

Be aware that the alarm output for power supply unit that are installed to the expansion backplanes will not work.

4.6.3.1 Watchdog Timer

The watchdog timer is a program error and hardware error detection timer. It goes ON when the scan time exceeds 640 ms.
When the watchdog timer is activated, at the same time the ALARM LED lights, the ALARM contacts on the power supply unit go ON, all outputs to the output units are turned OFF and the unit is put in halted state. (The system is in a non-processing state that includes communications with programming tools as well.)

Chapter 5

Procedure Until Operation

☞ next page

5.1 Before Turning ON the Power

5.1.1 Check Items

After wiring, be sure to check the items below before turning ON the power supply to the FP3/FP10SH system.

Item	Description
Unit mounting status	–Does the unit type match the device list during the design stage? –Are the unit mounting screws properly tightened? –Is the unit dust protected label detached?
Power supply unit	–Is power supply voltage supplied correctly? –For power supply units AFP3631 and AFP3638, are the voltage switch terminals shorted together for 100 to 120 V AC operation and open for 200 to 240 V AC operation? –Are the terminal block mounting screws properly tightened? –Is the wire size correct?
Input/Output units	–Does the wiring of connector and terminal match? –Is the operating voltage of I/O correct? –Are the terminal block mounting screws properly tightened? –Is the wire size correct?
Expansion cable	–Are the expansion cables properly connected?
Board number setting	–Are they set so that numbers are not identical? (If expansion backplane are used, the numbers for the board number set switch must be set.)
Setting of CPU	–Is the mode selector set to the PROG. mode? –Is the backup battery connector firmly connected? –Has the DIP switch of CPU been set correctly?
ROM mounting status	–Has the ROM been mounted in the correct direction? –Has the ROM been securely installed? Are the lead feet firmly secured and not likely to come loose? –For the FP3, does the ROM type match the position of device (ROM type) selector?

5.1.2 Procedure Up To Trial Operation

After installing and wiring, perform the trial operation by following procedure.

Procedure:

1. **Before turning ON the power, check the items described on the previous page**
2. **Turn ON the power**
3. **Check that the power supply unit's POWER LED and CPU's PROG. LED are ON**
4. **Enter the program**

   When using a programming tool, perform the operation "Clear Program" before inputting. Enter the program using the programming tool. Use the proramming tool's "total check function" to check for syntax errors.
5. **Check output wiring**

   Use the forced output function to check the output wiring.
6. **Check input wiring**

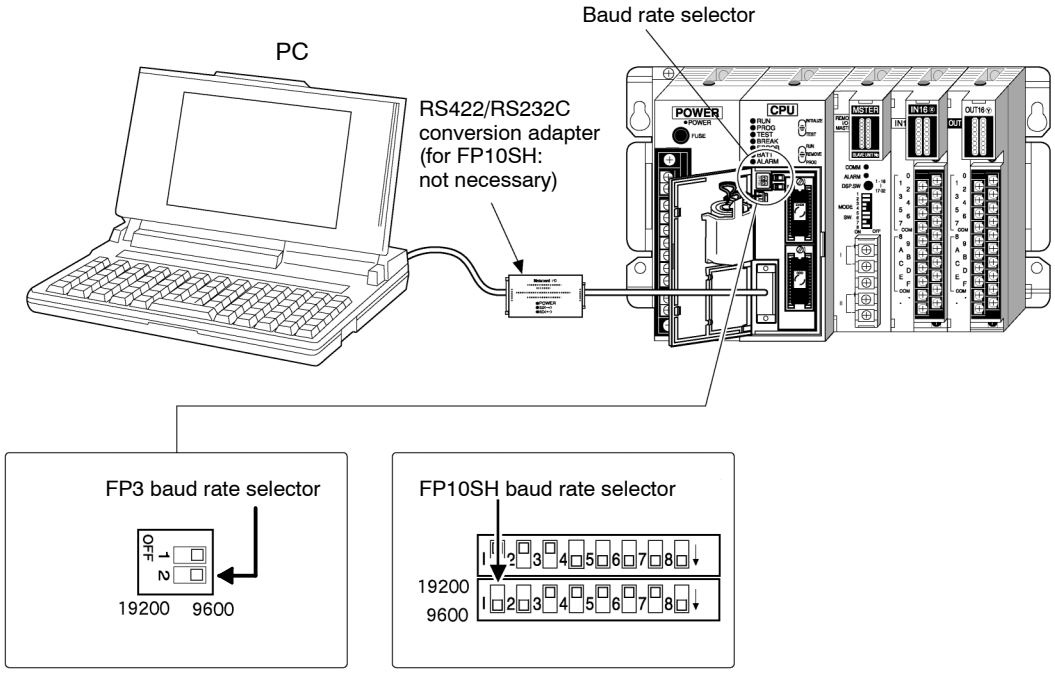
   Check the input wiring by watching the ON/OFF status of the input LEDs of input unit or by using the monitoring function of the programming tool.
7. **Switch the mode selector from PROG. to RUN mode**
8. **If the RUN LED turns ON, check the operation of the program**
9. **Edit the program (debug) if necessary**

   If there is an error in the operation, check the program using the monitoring function of the programming tool. And then correct the program.
10. **Save the edited program**

    We highly recommend to save the created program onto a floppy disk. Printing out is also possible.
    The program can also be saved on ROM for FP3 and on an IC memory card or ROM for FP10SH.

5.2 Programming with NPST−GR

5.2.1 Preparations



Connecting the FP3/FP10SH and a Computer

For FP3

An FP PC cable, RS422/RS232C conversion adapter (AFP8550) and commercially available RS232C cable are required to connect a personal computer to FP3.

For FP10SH

The RS232C cable (AFB85813) is required to connect a personal computer to FP10SH.

☞ **Note**

NPST−GR Ver 4. or later can be used with the FP10SH.

Setting the baud rate of CPU

Set the baud rate of the CPU using the baud rate selector of FP3 or operation condition switches (dip switches) of FP10SH.

Set the baud rate of the computer (NPST−GR) to match that of the CPU. (*section 5.2.2)

Computer settings

Set your personal computer's RS232C parameter to asynchronous. For the setting procedure, refer to the operation manual that came with your computer.

5.2.2 Configuring NPST−GR

Depending on the PLC type and communication speed (baud rate), it is necessary to set the basic configuration for NPST−GR. Be sure to set these items (parameters) before beginning programming.

SCREEN MODE
[MONO/COLOR]
Select either black−and−white (monochrome) or color for the display of the NPST−GR screen mode.

PLC TYPE
Select the PLC (programmable controller) type that is being used.

Communication format
The baud rate setting must match that of the CPU that is connected. (* section 5.2.1)

LOGGED DRIVE/DIRECTORY
Select the disk drive and directory from which the program and file are to be read.

NOTE DISPLAY
Select whether or not to display the title and the title is to be added to the filename when displaying the filename.

PROGRAMMING MODE
[Ladder symbol mode, Boolean ladder mode and Boolean non−ladder mode]
Select the inputting method for creating and editing the program.

5.2.2.1 Setting Method

Call up the “NPST CONFIGURATION” menu

1. Press the <ESC> key to display the “NPSTMENU.”
2. Select “1. NPST CONFIGURATION” from “NPST CONFIGURATION” and press the <ENTER> key. The “NPST CONFIGURATION” menu appears.

Set the configuration

Select the item to be set with the <↑> and <↓> keys.

PLC TYPE

1. Press the <ENTER> key. A list of the corresponding PLC (programmable controller) types appears.
2. Select PLC type with the <↑> and <↓> keys.

Select either “FP3 10K”, “FP3/FP–C 16K” or “FP10SH 30–120K” according to the information in the table below.

CPU type	Order number	Selection
FP3 CPU	AFP3210C–F and AFP3211C–F	FP3 10K
	AFP3220C–F	FP3/FP–C 16K
FP10SH CPU	AFP6211V3 and AFP6221V3	FP10SH 30–120K

NPST–GR Ver.3

```
FP1          0.9
FP1/FP-M   2.7k
FP1/FP-M     5k
FP3         10k
FP3/FP-C    16k
FP5         16k
FP10/FP10S  30k
FP10        60k
```

NPST–GR Ver.4

```
FP0        2.7k
FP0          5k
FP1         0.9
FP1/FP-M   2.7k
FP1/FP-M     5k
FP3         10k
FP3/FP-C    16k
FP5         16k
FP5         24k
FP10/FP10S  30k
FP10        60k
FP10SH 30-120k
```

3. Press the <ENTER> key. The selected PLC (programmable controller) type appears.

Log the setting items (parameters)

After setting the items (parameters), log the settings following the procedure below.

Procedure:

1. **Press the <F1> key. The confirmation screen below appears.**

   "LOG PARAMETERS? [Y/N]"

   "SAVE DISK? [YES/NO]"

2. **Verify that there are no mistakes in the settings. If there is a mistake, press the <N> key and set the parameters correctly.**

3. **Select whether or not to write the settings to disk with <←> and <→> keys. If you select [YES], then the new parameters will take effect the next time the power is turned ON.**

4. **Press the <Y> key. The settings are logged. If you selected [YES] in step 3., then the message below appears.**

   "SAVEING TO THE DISK COMPLETED."

Completion of configuration setting

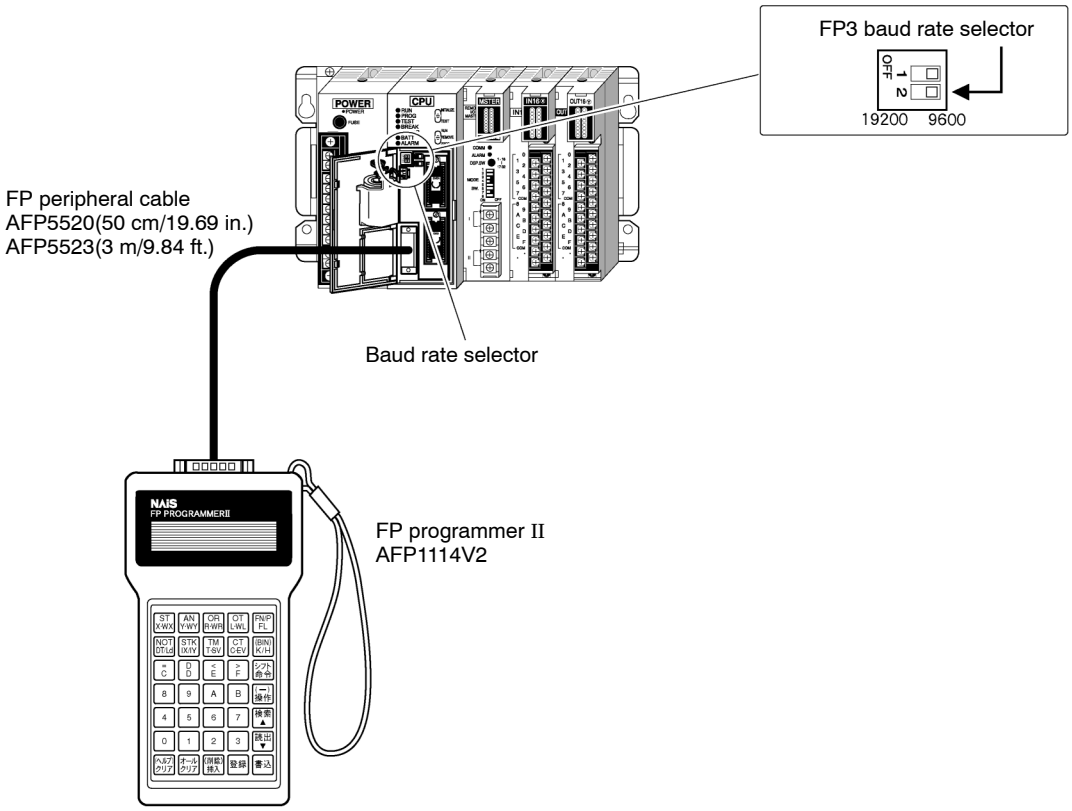
Procedure:

Press the <ESC> key to complete the configuration settings. The following message will appear if the settings are not recorded. If it is necessary to record the settings, press the <N> key and proceed from step 3. If it is not necessary to record the settings, press the <Y> key to complete the settings.

"EXIT OK? (Y/N)"

5.3 Programming with an FP Programmer II

5.3.1 Preparations



Connecting the FP3 and an FP programmer II
An FP peripheral cable is required to connect an FP3 to an FP programmer II.

– FP peripheral cable :
  50 cm/19.69 in (AFP5520)
  3 m/9.84 ft. (AFP5523)

Setting the baud rate of the CPU
Set the baud rate of CPU using the baud rate selector.
When using the FP programmer II, a baud rate of either 9,600 bps or 19,200 bps can be selected.

Storage location of programs
The programs input with the FP programmer II are stored one after another in the FP3's built-in memory (RAM).

Downloading a program

Procedure:

1. **Connect FP programmer II and the FP3 CPU using the FP peripheral cable.**
2. **Set the mode selector of the CPU to PROG.**
3. **Press the keys on the FP programmer II, as shown below, to clear all the data stored.**

   [ACLR] [(–) OP] [0] [ENT] [SHIFT SC] [(DELT) INST]

4. **Enter the address from where you want to enter instructions. Use the alphanumeric keys to enter the address. In the example, instructions are entered from address 0, therefore, press [ACLR] [0] [READ ▼] to read its contents.**
5. **Download the program to the FP3 CPU.**

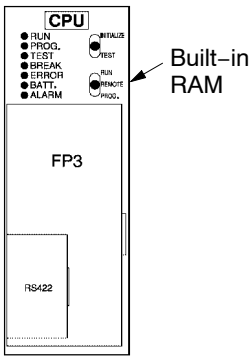
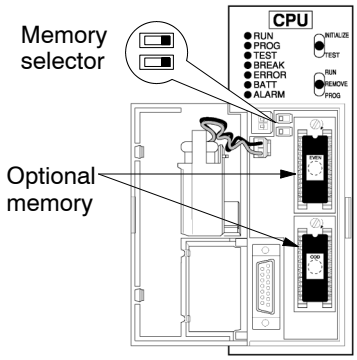
☞ Notes

- **An alarm will sound if you try to download a program while in RUN mode or if you press the wrong keys. If an alarm sounds, press the [ACLR] key and redo the download operation from the beginning.**
- **The first time you input a program, be sure to execute the program clear procedure (step 3, above) before starting input.**
- **Previous FP programmers (AFP1111A, AFP1112A, AFP1111 and AFP1112) cannot be used with the FP10SH.**

5.4 Operation of FP3

5.4.1 RAM and ROM Operations

5.4.1.1 Comparison of RAM and ROM Operations

Item	RAM operation	ROM operation
Operating method	 The FP3 CPU operates using built–in RAM. Have the memory selector set to the RAM position.	 The optional memory (EPROM or EEPROM) is installed for ROM operation. Have the memory selector set to the ROM position.
Execution of program	The program written into the RAM is executed.	When the mode is changed from PROG. mode to RUN mode, if the power is turned ON while the in the RUN mode, the program written into the ROM are loaded into the RAM and the program is executed.
Memory backup during a power failure	The program, system register, operation memory, and other data, that is stored in the RAM are saved using a backup battery.	Since the program and system registers are written into the ROM, backup is not necessary. Since the hold type data of the operation memory is written into the RAM, backup is necessary using the backup battery.
Maintenance	It is necessary to replace the backup battery when voltage is low.	If a program does not use the hold type data of the operation memory, then operation without being connected to the backup battery is possible.
Miscellaneous (options)	Options are unnecessary.	Optional memory (EPROM or EEPROM) is necessary. If you are using the EPROM, a commercially available ROM writer is necessary for writing.

5.4.2 Holding the Data During Power Failure

5.4.2.1 Backup of Operation Memory

The internal relay, data registers and other hold type data are backed up by the battery. When performing ROM operation with the internal relay, data registers, and other such data set to non– hold type data, you can perform operation without being connected to a backup battery.

5.4.2.2 Setting the Battery Error Warnings

With the exception of FP3 CPU version 4.4 or greater, if the CPU is set with the battery error warning disabled, the ERROR LED does not light even if operating while not being connected to a backup battery. Set the battery error warning according to the following procedure:

Procedure:

For NPST–GR software

1. **Press the <ESC> key to display the [NPST MENU]. In the [NPST MENU] screen, select the [SYSTEM REGISTER] option from the [PLC CONFIGURATION] and press <ENTER> key.**
2. **In the [PLC CONFIGURATION] screen, press the <F8> key and select the [ACT ON ERROR] option. Then set the [BATTERY ERROR] to [DISABLE].**
3. **Press the <F1> key to save the setting contents.**
4. **Press the <ESC> key and then the <Y> key to return to the original screen.**

For FP Programmer II

1. **Use the following key sequence for the system register**

   (–) OP | 5 | 0 | ENT

2. **To read contents of system register 4 , press the following keys**

   4 | READ B

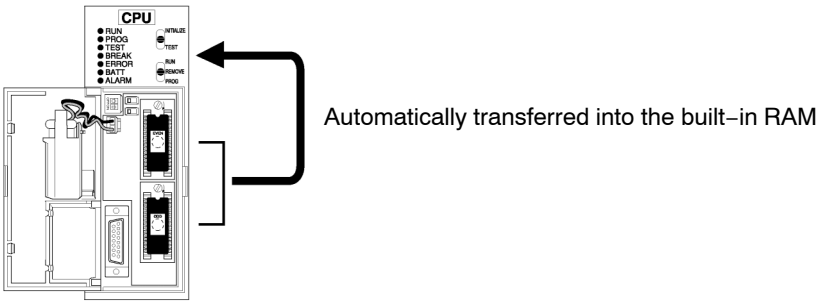
3. **To disable the battery error warning, press the following keys.**

   ACLR | 1 | WRT

5.4.3 Precautions for ROM Operation

Once the ROM has been installed, be aware that operation varies as described below, depending on the position of the memory selector when the power supply is turned ON.

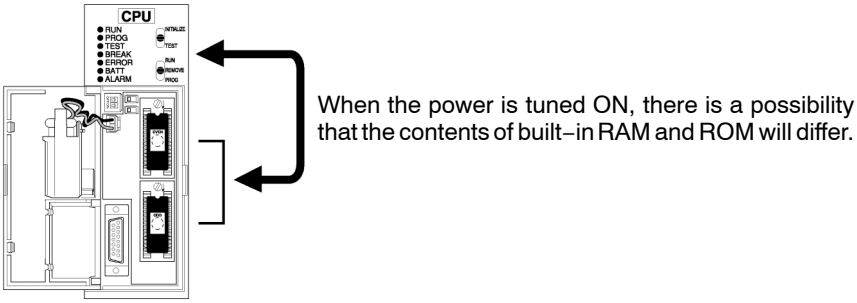
Power is turned ON with the memory selector set to ROM position
When the power is turned ON, the contents of the memory (ROM) is automatically transferred into the built–in RAM. Note that the previous contents of the RAM will be erased.



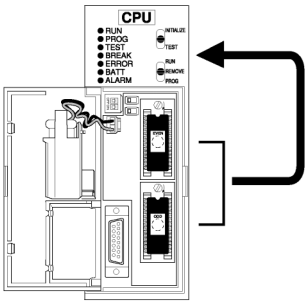
Power is turned ON with the memory selector set to RAM position
Even if the memory (ROM) is installed, the programming tools read the contents of the built–in RAM.

In order to verify the contents of the memory (ROM), you can transmit the contents to the built–in RAM using your programming tool (* section 5.4.3.1).

To then perform ROM operation, turn the power OFF, set the memory selector to the ROM position. And then the power is turned ON and restart the system.



5.4.3.1 Transfer Data From ROM to the Built–in RAM



Procedure:

Using NPST–GR software

1. **Press the <CTRL> and <ESC> keys together to switch to the online monitor mode.**
2. **Press the <ESC> key to display the [NPST MENU]. Select the [COPY PROGRAM BETWEEN ROM & RAM] option from the [PROGRAM MANAGER] menu. And then press the <ENTER> key.**
3. **After verifying that the menu reads [COPY ROM TO RAM]. Press the <F1> key.**

Using FP programmer II

Press the following key operations.

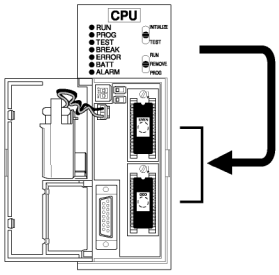
ACLR (–) OP 9 0 ENT WRT

5.4.4 Writing to ROM

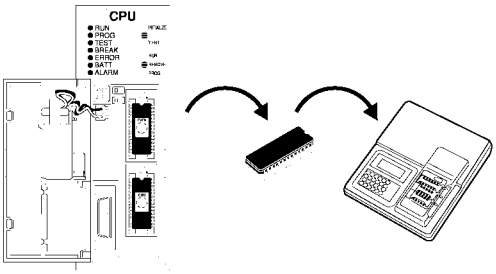
5.4.4.1 Using a Commercially Available ROM Writer Via EEPROM

Procedure:

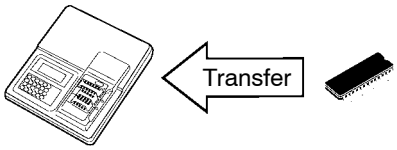
1. **Turn OFF the power and attach the master memory (EEPROM) to the CPU.**
   Set the device (ROM type) selector to the EEPROM position.
2. **Verify that the mode selector is set to PROG. mode and then turn ON the power.**
3. **When using the NPST−GR or FP programmer II, transfer the contents of the built−in RAM to the master memory (EEPROM). (* refer to the next page)**



4. **Turn OFF the power, and detach the programmed master memory (EEPROM) from the CPU and attach it in the commercially available ROM writer.**

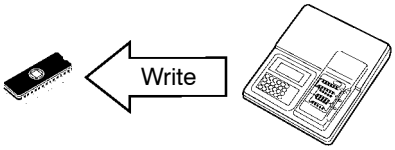


5. **Transfer the contents of master memory (EEPROM) to the ROM writer**



☞ next page

6. **Remove the master memory (EEPROM) and install the memory (EPROM) and write the contents of the ROM writer to the memory (EPROM).**



☞ **Note**

Refer to the manual of commercially available ROM writer for operation procedure and setting of ROM.

Transfer data from the built–in RAM to master memory (EEPROM)

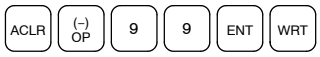
Procedure:

Using NPST–GR software

1. **Press the <CTRL> and <ESC> keys together to switch to the online monitor mode.**
2. **Press the <ESC> key to display the [NPST MENU]. Select the [COPY PROGRAM BETWEEN ROM & RAM] option from the [PROGRAM MANAGER] menu. And then press the <ENTER> key.**
3. **Press the <F2> key to switch to [COPY RAM TO ROM].**
4. **Press the <F1> key. The contents of the built–in RAM are transfered to EEPROM.**

Using the FP programmer II

Press the following key operations.



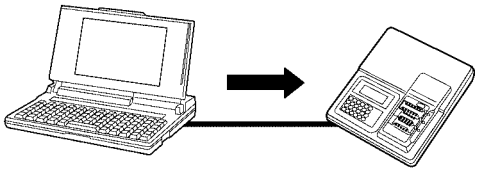
☞ **Note**

If you want to write the contents of built–in RAM of the FP3 to the master memory (EEPROM), be sure to verify that the memory selector is set to the RAM position before turning ON the power.

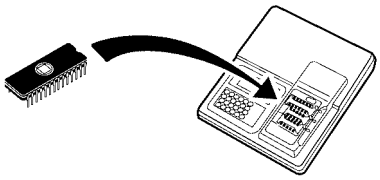
5.4.4.2 Using NPST–GR and a Commercially Available ROM Writer

Procedure:

1. **In the NPST–GR at the computer, select the [LOAD TO/FROM ROM WRITER] option to transfer the program to the commercially available ROM writer.**



2. **Attach the memory (EPROM) in the commercially available ROM witer.**
   Write the data to the memory (EPROM) with the commercially available ROM writer.



☞ **Note**

Refer to the manual for the commercially available ROM writer for the proper settings.

Transfer program from the computer with NPST–GR to the ROM writer

Procedure:

1. **In the [NPST CONFIGURATION] menu, press the <SHIFT> and <F6> keys together to display the [ROM CONFIG].**

```
<ROM CONFIG> window
    TRANS RATE (bps)  [ 9600 Σ 4800 Σ 2400 Σ 1200 Σ 600 Σ 300 ]
    DATA LENGTH       [ 8 Σ 7 ]
    PARITY CHECK      [ NO Σ EV Σ OD ]
    STOP BIT          [ 1 Σ 2 ]
```

☞ next page

2. Set the transmission rate and communication format that matches that for the ROM writer with, and press <F1> key to save the settings.

3. Press the <ESC> key, and select [PROGRAM MANAGER] from the [NPST MENU] then select the [LOAD TO/FROM ROM WRITER] option. Press the <ENTER> key.

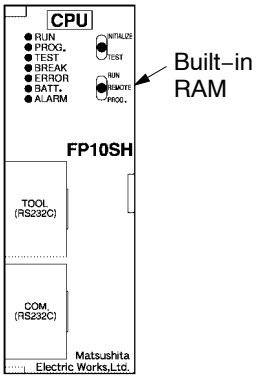
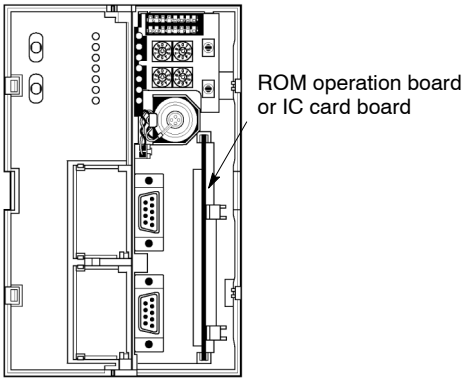
```
[LOAD TO/FROM ROM WRITER]
    READ    WRITE    VRFY
  INTEL HEX          MOTOROLA [S]
  SERIAL PORT  CENTRNICS PORT    FILE
  NO PASSWORD        WITH PASSWORD
F1  : EXECUTE.
```

4. Specify the transmission format and connection method appropriate for the ROM writer and then select [WRITE]. Press the <F1> key. The program is transfered to the ROM writer.

5.5 Operation of FP10SH

5.5.1 RAM, ROM and IC Memory Card Operations

5.5.1.1 Comparison of RAM, ROM and IC Memory Card Operation

Item	RAM operation	ROM operation	IC memory card operation
Operating method			
	This operates based on built-in RAM of CPU. Set the program memory switch (SW5) to OFF (* section 2.5.1.4).	The optional ROM operating board is installed for ROM operation. Set the program memory switch (SW5) to ON. (* section 2.5.1.4).	The optional IC memory card and IC card board are installed for IC memory card operation. Set the program memory switch (SW5) to ON. (* section 2.5.1.4).
Execution of program	The program written into the RAM is executed.	When the power is turned ON, the program written into ROM are transferred into the RAM and the program is executed.	Turning the power ON will transferred the program (file named AUTOEXEC. SPG) of the IC memory card into the RAM and execute the program. Using the **F14 (PGRD)**/**P14 (PPGRD)** instructions, it is possible to read out the program (with an arbitrary file name) stored in the IC memory card.

☞ next page

Item	RAM operation	ROM operation	IC memory card operation
Memory backup during a power failure	The program, system register and operation memory that is stored in the RAM are saved using the backup battery.	Since the contents of program and the system register are written to the ROM, backup is not necessary. Since the hold type data of the operation memory is written to the RAM, it is backed up by the backup battery.	As the program and the contents of the system registers are written onto the IC memory card, backup is not necessary. As the hold type data of the operation memory is written to the RAM, backup is necessary by the backup battery.
Maintenance	It is necessary to replace the backup battery when voltage is low.	If a program does not use the hold type data of the operation memory, it is possible to operate without being connected to the backup battery.	If the program does not use the hold type data of the operation memory, it is possible to operate without the backup battery (when using the SRAM type IC memory card, it is necessary to replace the battery of the IC memory card.).
Miscellaneous (options)	Options are unnecessary.	The optional ROM operation board and either the EPROM or FROM is necessary. If you are using the EPROM, a commercially available ROM writer is necessary for writing. The NPST−GR version 4.2 or greater is necessary.	The optional IC memory card and IC card board are necessary.

5.5.2 Holding the Data During Power Failure

5.5.2.1 Backup of Operation Memory

The internal relay, data registers and other hold type data are backed up by the battery.

When performing ROM operation or IC memory card operation with the internal relay, data registers, and other such data set to non– hold type data, you can perform operation without being connected to a backup battery.

5.5.2.2 Setting the Battery Error Warnings

If the FP10SH CPU is set with the battery error warning disabled using system register 4, the ERROR LED does not light even if operating while not being connected to a battery.
Set the battery error warning according to the following procedure:

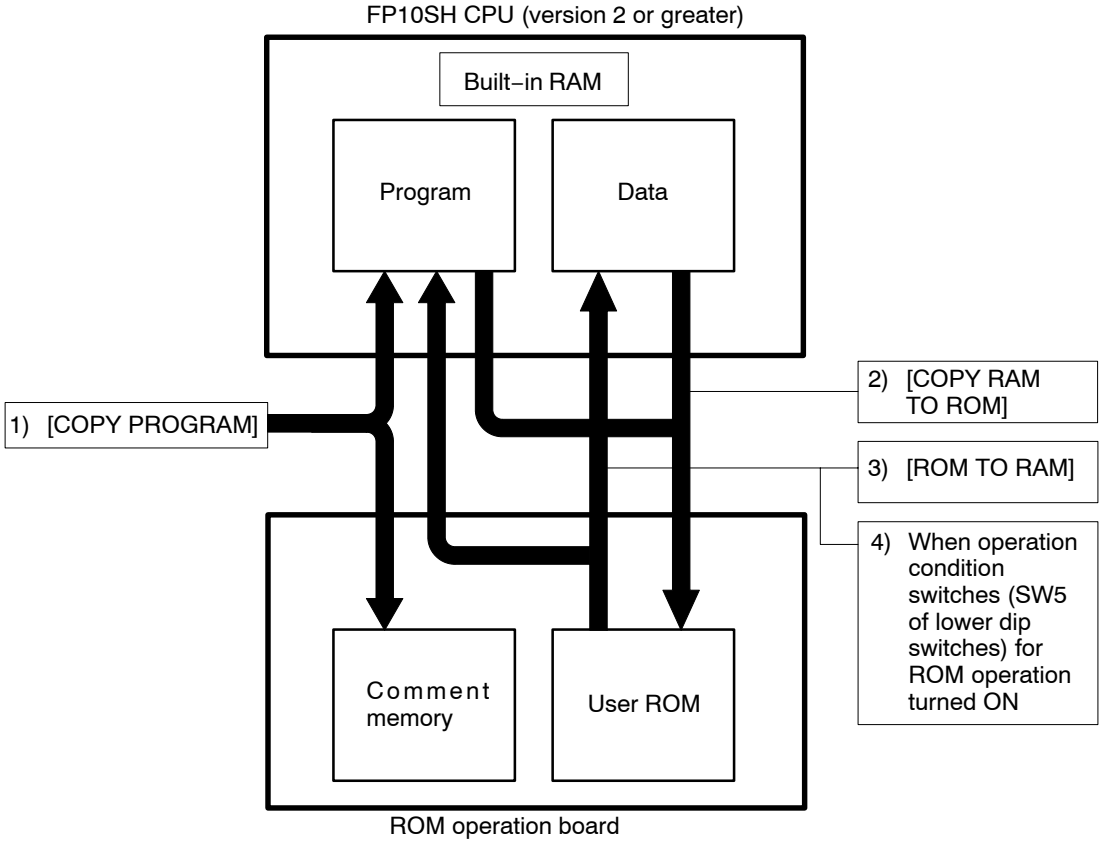
Procedure:

- **For NPST–GR software**

  1. **Press the <ESC> key to display the [NPST MENU]. In the [NPST MENU] screen, select the [SYSTEM REGISTER] option from the [PLC CONFIGURATION] and press the <ENTER> key.**
  2. **In the [PLC CONFIGURATION] menu, press the <F8> key and select the [ACT ON ERROR] option. Then set the [BATTERY ERROR] to [DISABLE].**
  3. **Press the <F1> key to save the setting contents.**
  4. **Press the <ESC> key and then the <Y> key to return to the original screen.**

5.6 How To Use a ROM Operation Board (for FP10SH only)

5.6.1 Overview of FP10SH ROM Operation Board



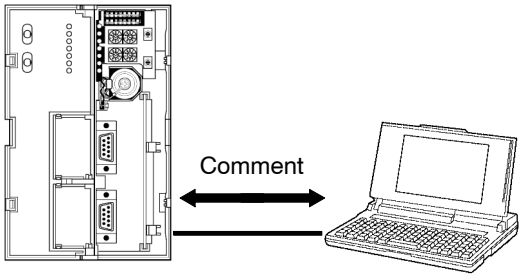
1) You can copy programs and comments into the FP10SH using [COPY PROGRAM] in the NPST−GR. At this time, the program is stored in the built−in RAM of the FP10SH and the comment is stored in the comment memory of the ROM operation board. (* section 5.6.2)
2) You can copy programs and data of the built−in RAM of the FP10SH into the user ROM of ROM operation board using [COPY RAM TO ROM] in the NPST−GR. (* section 5.6.4)
3) You can copy programs and data in the user ROM of ROM operation board into the built−in RAM of the FP10SH using [ROM TO RAM] in the NPST−GR. (* section 5.6.3)
4) Turning ON the power when the operation condition switches (SW5 of lower dip switches) is ON, will automatically transfer the program and data stored in the user ROM of ROM operation board into the built−in RAM of the FP10SH (* section 5.6.3).

5.6.2 Function of ROM Operation Board

5.6.2.1 Comment Storager Function

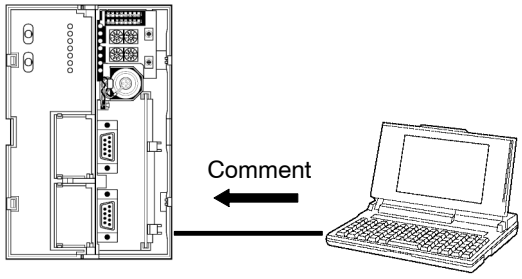
The comment storage function has been added to the FP10SH. Use NPST−GR version 4 to store the comments to the ROM operation board.

There are three types of comments: the line space comment, the comment sentence and I/O comment.



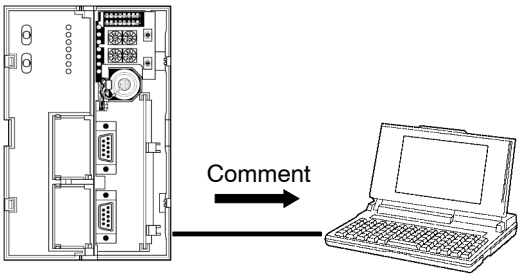
Storage to user ROM

With NPST−GR version 4.2 or greater, by selecting the [PROG & I/O CMT] of the [LOAD A PROGRAM TO PLC] menu, the program on the NPST−GR is automatically compressed and stored in the built−in RAM of FP10SH CPU and the comment is automatically compressed and stored in the comment memory inside the user ROM of the ROM operation board.



Reading from the user ROM

Select the [PROG & I/O CMT] option of the [LOAD A PROGRAM FROM PLC] menu to read the built−in RAM and the data of the comment memory to the NPST−GR.



5.6.2.2 Precautions for Comment Storage

To erase data in the comment memory on the ROM operation board, select the [PROG & I/O CMT] option of the program erase function of NPST−GR.

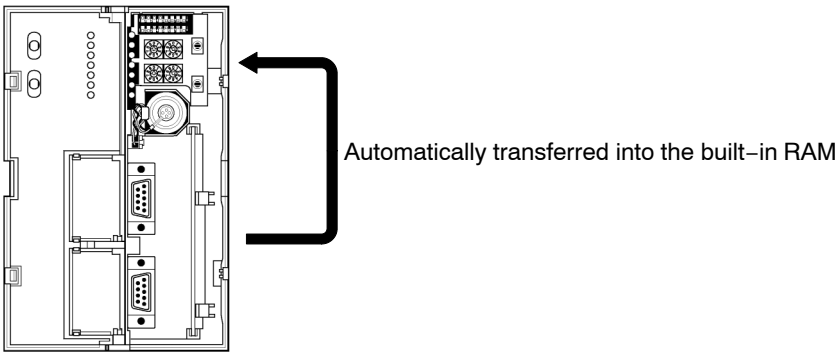
When storing the after compressing the comment, approximately 1MB of comment can be stored. Otherwise, approximately 256kB of comment can be stored.

To compress the comment data, you must have the compression software LHA in the current directory and 530kB of open area in the main memory.

5.6.3 Precautions for ROM Operation

Once the ROM has been installed, be aware that operation varies as described below, depending on the position of the program memory selector when the power supply is turned ON.

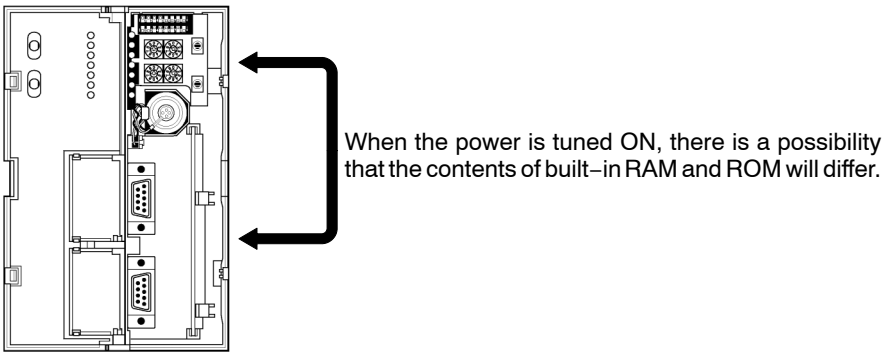
Power is turned ON with program memory selector set to ON (ROM) position
When the power is turned ON, the contents memory (ROM) is automatically transferred into the built–in RAM. Note that the previous contents of the RAM will be erased.



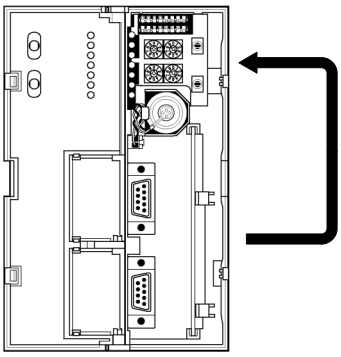
Power is turned ON with program memory selector set to OFF (RAM) position
Even if the memory (ROM) is installed, the programming tools read the contents of the built–in RAM.

In order to verify the contents of the memory (ROM), you can transmit the contents to the built–in RAM using your programming tool (* section 5.6.3.1).

To then perform ROM operation, turn the power OFF, set the memory selector to the ON (ROM) position. And then the power is turned ON and restart the system.



5.6.3.1 Transfer Data From ROM to the Built–in RAM



Procedure:

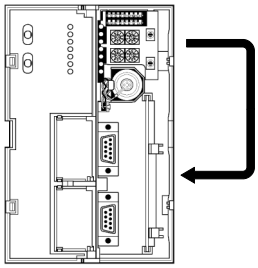
Using NPST–GR software

1. **Press the <CTRL> and <ESC> keys together to switch to the online monitor mode.**
2. **Press the <ESC> key to display the [NPST MENU]. Select the [COPY PROGRAM BETWEEN ROM & RAM] option from the [PROGRAM MANAGER] menu. And then press the <ENTER> key.**
3. **After verifying that the menu reads [COPY ROM TO RAM]. Press the <F1> key.**

5.6.4 Transfer Data from RAM to FROM

5.6.4.1 Method for Transferring From RAM to FROM

Select the [COPY RAM TO ROM] function in the [PROGRAM MANAGER] function of NPST−GR to transfer the program and data of the CPU to the ROM. You can specify the start and end address for each area WL, WR, DT, FL, SV, EV, and LD.



Procedure:

Using NPST−GR software

1. **Press the <CTRL> and <ESC> keys together to switch to the online monitor mode.**
2. **Press the <ESC> key to display the [NPST MENU]. Select the [COPY PROGRAM BETWEEN ROM & RAM] option from the [PROGRAM MANAGER] menu. And then press the <ENTER> key.**
3. **Press the <F2> key to switch to [COPY RAM TO ROM]**
4. **Press the <F3> key to call up switch on the menu, and specify the start and end address of the data file.**
5. **Press the <F1> key to transfer.**

5.6.4.2 Storage Capacity of User ROM

The potential storage capacity of user ROM is:

Program capacity (Number of program step)
Data capacity (Total data file capacity)
\+ System register capacity (Fixed value: 2 k words)

Total number of words

The largest number potential value of the above is 127 k words.

5.6.4.3 Precautions for Comment Storage

Editing of the program cannot be done during ROM operation. Transfer the data after turning the program memory selector OFF. (* section 5.6.5.1)

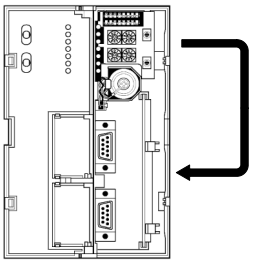
5.6.5 Writing to ROM

It is possible to write to the master memory (Flash ROM: AFP5208) when it is installed in the CPU, however the memory (EPROM: AFP5209) cannot be written with anything other than a commercially available ROM writer.

5.6.5.1 Writing of Master Memory (FROM) and Memory (EPROM)

Procedure:

1. **Turn the power OFF and install the ROM operation board installed with the master memory (FROM). Turn OFF the operation condition switches (program memory selector: lower dip switches SW5) of CPU.**
2. **Verify that the PROG. mode has activated and turn the power ON.**
3. **Using the NPST−GR, transfer the contents of the built−in RAM to master memory (FROM). (* [COPY PROGRAM BETWEEN ROM & RAM])**
4. **When performing ROM operation, set the operation condition switches (program memory selector: lower dip switches SW5) of the CPU to ON, and then turn the power ON.**



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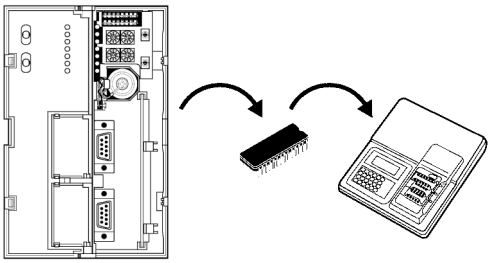
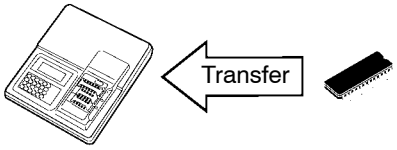
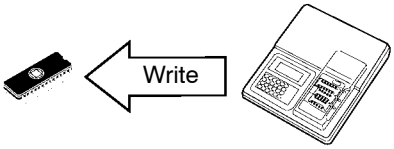
5. Turn the power OFF and detach the master memory (FROM) from the CPU. Attach it to the commercially available ROM writer.



6. Transfer the contents of master memory (FROM) to the ROM writer.



7. Detach the master memory (FROM) and attach the memory (EPROM) and begin writing.



☞ **Notes**

- **Refer to the commercially available ROM writer manual regarding the setting and writing method. If a passwords is on the CPU, it is possible to create a password for master memory.**
- **When writing the contents of the FP10SH built–in RAM to master memory (FROM), be sure to verify that the operation condition switches (program memory selector: lower dip switches SW5) is OFF position before turning the power ON.**

Transfer using the NPST–GR software

Use the [LOAD TO/FROM ROM WRITER] option of NPST–GR version 4.2 or later to directly transfer the commercially available ROM writer.

Procedure:

1. **In the [NPST CONFIGURATION] menu, press the <SHIFT> and <F6> keys to display the [ROM CONFIG].**

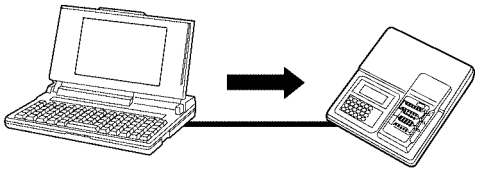
```
<ROM CONFIG> Window
    TRANS RATE (bps)  [ 9600 Σ 4800 Σ 2400 Σ 1200 Σ 600 Σ 300 ]
    DATA LENGTH       [ 8 Σ 7 ]
    PARITY CHECK      [ NO Σ EV Σ OD ]
    STOP BIT          [ 1 Σ 2 ]
```

2. **Set the transmission rate and communication format that matches that for the ROM writer with, and press <F1> to save the settings.**

3. **Press the <ESC> key, and select [PROGRAM MANAGER] from the [NPST MENU] then select the [LOAD TO/FROM ROM WRITER] option. Press the <ENTER> key.**

```
[LOAD TO/FROM ROM WRITER]
    READ    WRITE    VRFY
    INTEL HEX        MOTOROLA [S]
    SERIAL PORT      CENTRNICS PORT    FILE
    NO PASSWORD      WITH PASSWORD
F1  : EXECUTE.
```

4. **Specify the transmission format and connection method appropriate for the ROM writer and then select [WRITE]. Press the <F1> key. The data is transfered to the ROM writer.**



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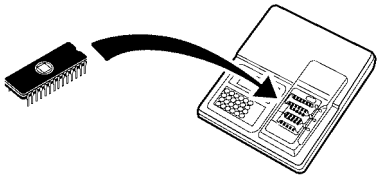
5. Attach the memory to the commercially available ROM writer. Write the data to the memory with the ROM writer.

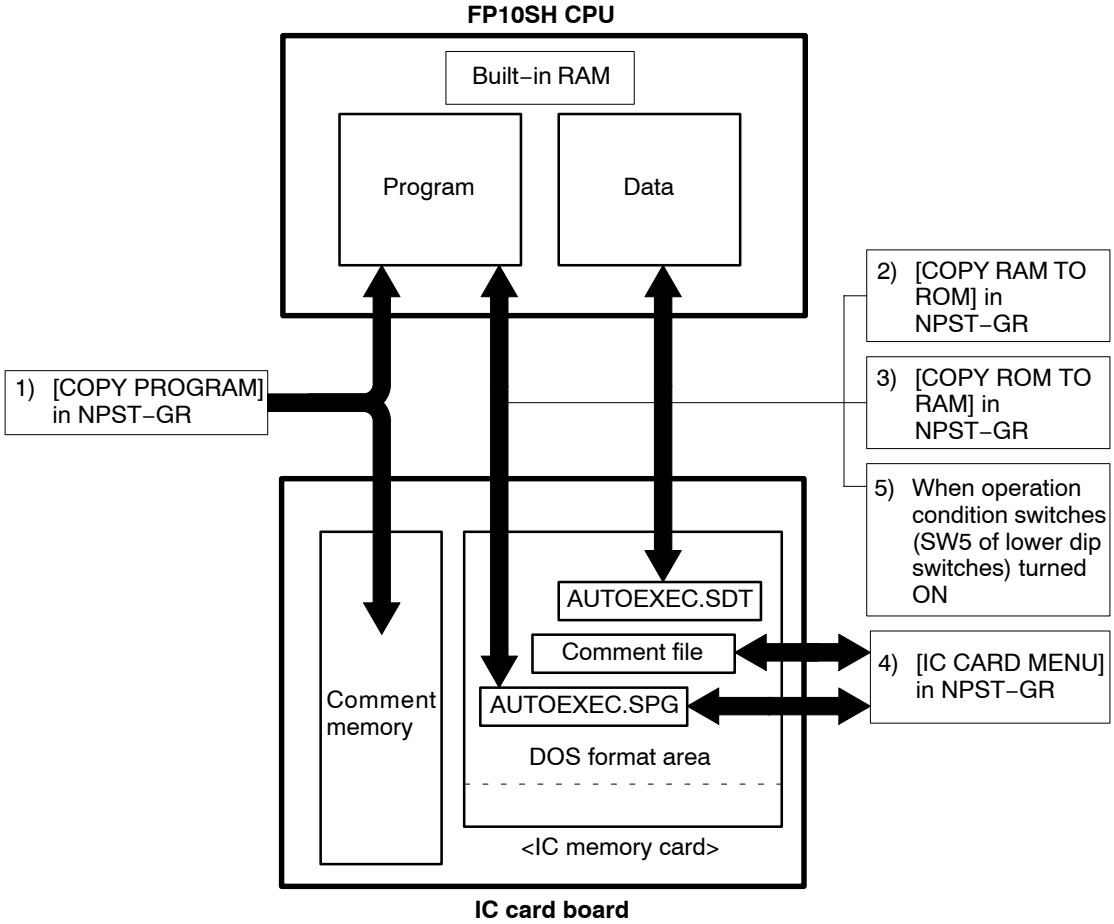


☞ **Note**

Refer to the commercially available ROM writer manual regarding the setting and writing method. If a passwords is on the CPU, it is possible to create a password for master memory.

5.7 How To Use IC Card Board (for FP10SH only)

5.7.1 Overview of FP10SH IC Card Board



1) You can copy programs and comments an be written into the FP10SH using [COPY PROGRAM] in the NPST–GR. At this time, program is stored in the built–in RAM of the FP10SH and the comment is stored in the comment memory of the IC card board. (* section 5.7.2).

2) The program and data of the built–in RAM of the FP10SH can be written into the DOS format area of the IC memory card using [COPY RAM TO ROM] in the NPST–GR. (* section 5.7.2.3).

3) You can copy the program and data in the DOS format area of the IC memory card is written into the built–in RAM of the FP10SH using [COPY ROM TO RAM] in the NPST–GR. (* section 5.7.3).

. next page

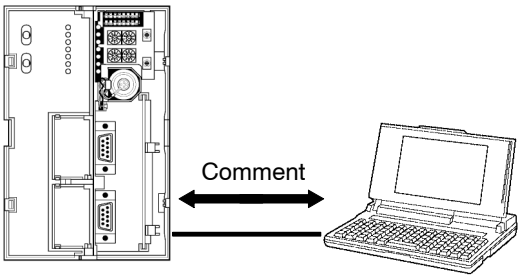
4) You can program and comment on the floppy disk or hard disk is written into the DOS format area of the IC memory card using [IC CARD MENU] in the NPST−GR. (* section 6.2)

5) If the power is turned ON with the operation condition switches (SW5 of lower dip switches, program memory selector) set to ON, the program and data in the DOS format area of the IC memory card automatically transfer into the built−in RAM FP10SH. (* section 5.7.3).

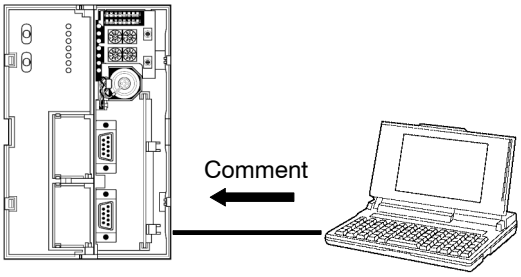
5.7.2 Function of IC Card Board

5.7.2.1 Comment Storage Function

The comment storage function has been added to the FP10SH. Use NPST−GR version 4 to store the comments to the IC memory card.
There are three types of comments: the line space comment, the comment sentence and I/O comment.



Storage to IC memory card
With NPST−GR version 4.2 or greater, by selecting the [PROG & I/O CMT] of the [LOAD A PROGRAM TO PLC] menu, the program on the NPST−GR is automatically compressed and stored in the built−in RAM and the comment is automatically compressed and stored that uses the comment memory of the IC memory card.

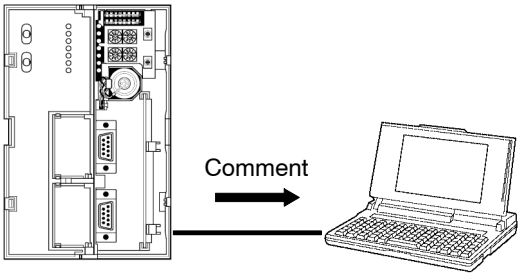


☞ **Note**

The IC card board (AFP6209A) has a built−in 512kB comment storage memory.

Reading from IC memory card

Select the [PROG & I/O CMT] option of the [LOAD A PROGRAM FROM PLC] memu to read the data of the built−in RAM and the comment memory to the NPST−GR.



5.7.2.2 Precautions for Comment Storage

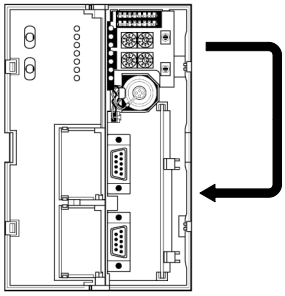
To erase data in the comment memory on the IC memory card, select the [PROG & I/O CMT] option of the program erase function of NPST−GR.

When storing the after compressing the comment, approximately 2MB of comment can be stored. Otherwise, approximately 512kB of comment can be stored.

To compress the comment data, you must have the compression software LHA in the current directory and 530kB of open area in the main memory.

5.7.2.3 Transfer Data from RAM to IC Memory Card

Select the [COPY RAM TO ROM] option in the NPST−GR [PROGRAM MANAGER] menu to transfer the program and data of the CPU to the IC memory card. Specify the start and end address for each area WL, WR, DT, FL, SV, EV, and LD.



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Type of file created by the IC memory card

Type	File name	Description
Program	AUTOEXEC.SPG	Program automatic start up
Data	AUTOEXEC.SDT	Readable and editable with the NPST–GR data register edit function

☞ **Note**

If the stored data exceeds 25,472 words it becomes a AUTOEXEC.LDT data file.

5.7.2.4 Precautions for Data File Creation

Data files cannot be created with the IC card menu of NPST–GR, data register edit function or **F14 (PGRD)**/**P14(PPGRD)** instructions.

Refer to section 6.2.4 for the data storage capacity of IC memory card.

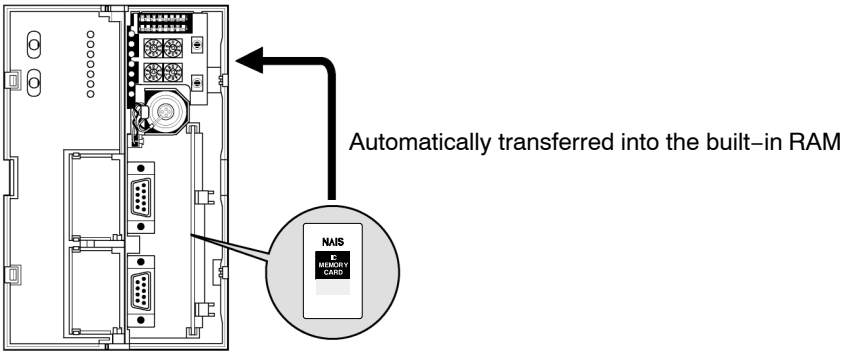
Procedure:

1. **Press the <CTRL> and <ESC> keys together to switch to the online monitor mode.**
2. **Press the <ESC> key to display the [NPST MENU]. Select the [COPY PROGRAM BETWEEN ROM & RAM] option from the [PROGRAM MANAGER] menu. And then press the <ENTER> key.**
3. **Press the <F2> key to switch to [COPY RAM TO ROM].**
4. **Press the <F3> key to call up switch on the menu, and specify the start and end address of the data file.**
5. **Press the <F1> key to transfer.**

5.7.3 Precautions for IC Memory Card Operation

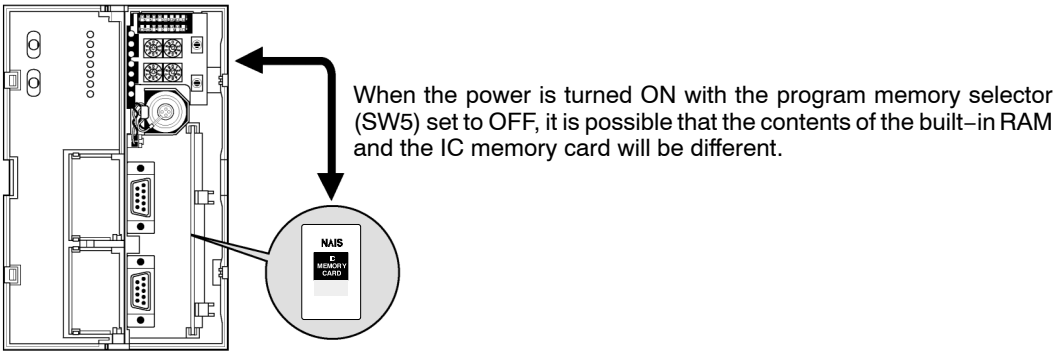
Once the IC memory card has been installed, be aware that operation varies as described below, depending on the position of the program memory selector (SW5 of lower dip switches) of operation condition switch when the power is turned ON.

Power is turned ON when program memory selector (SW5) of operation condition switches set to ON position.
When the power is turned ON, the program file name <AUTOEXEC> of the IC memory card is automatically transferred into the built−in RAM. Note that the previous contents of the RAM will be erased.



Power is turned ON when program memory selector (SW5) of operation condition switches set to OFF position.
Even if the IC memory card is installed, the programming tool read the contents of the built−in RAM.

When operating the program that is written into the IC memory card, set the program memory selector (SW5) of the operation condition switches to ON position and then the power is turned ON and restart the system.



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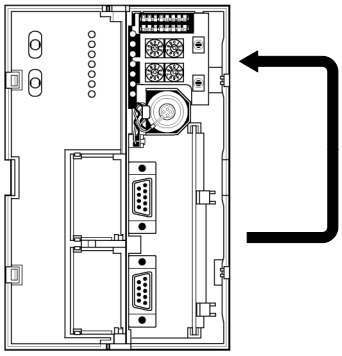
☞ **Notes**

- **Refer to chapter 6 for details about how to write to the program to the IC memory card.**
- **Refer to section 2.5.1.4 for details about how to set the operation condition switches.**

5.7.3.1 Transfer Data From IC Memory Card To Built–in RAM



Procedure:

Using NPST–GR software

1. **Press the <CTRL> and <ESC> keys together to switch to the online monitor mode.**
2. **Press the <ESC> key to display the [NPST MENU]. Select the [COPY PROGRAM BETWEEN ROM & RAM] option from the [PROGRAM MANAGER] menu. And then press the <ENTER> key.**
3. **After verifying that the menu reads [COPY ROM TO RAM] and press the <F1> key.**

5.7 How To Use IC Card Board (for FP10SH only)

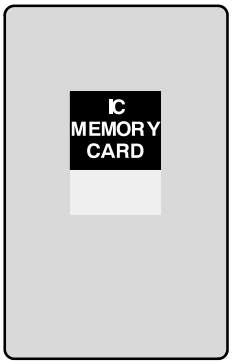
Chapter 6

IC Memory Card

6.1 Overview of IC Memory Card

The IC memory card is optional memory to be used with the FP10SH. It is not for use with the FP3. It has two main purposes, saving programs and expanding the data area memory. One IC memory card has the following three main applications:

- Exclusively for use in program storage
- Exclusively for use in expanding data memory area
- For combined use in program storage and expanding data memory area



For use in program storage
The program is written and saved onto the IC memory card. The IC memory card writted program is then used as the program memory.
With the NPST–GR, change the name of the file to [AUTOEXEC] and make a copy of the file. Then, by turning the power ON while the program memory selection (SW5) of the operation condition switch is set to ON position (IC memory card), the program automatically loads into the built–in RAM and you can begin operation.

Execute the **F14 (PGRD)**/**P14 (PPGRD)** instruction during RUN and it is possible to switch the program with the program of any specified file name.

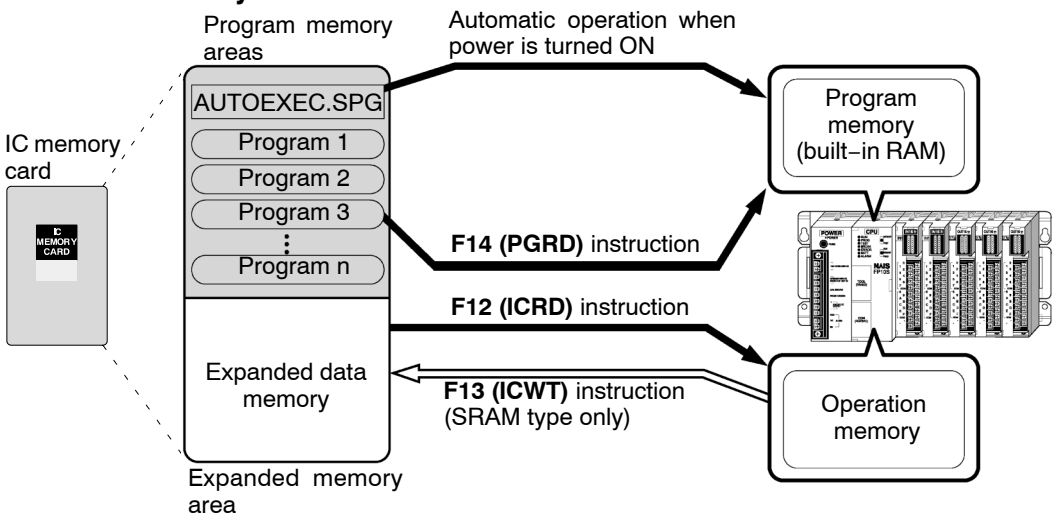
For use in expanding data memory area
Such things as the data written in the data register of FP10SH are written to the IC memory card. With this method, the IC memory card can be used as an expanded memory area can be used for the writing and reading of data by program.
When writing data, use the **F13 (ICWT)**/**P13 (PICWT)** instruction and when reading data from IC memory card, use the **F12 (ICRD)**/**P12 (PICRD)** instruction.

The FLASH–EEPROM type IC memory card is exclusively for reading.

☞ **Note**

The IC memory card of SRAM type and FLASH–EEPROM type are split into two areas, one for program storage and one for expanding data memoy.

How the IC memory card is used



When using the IC memory card as program memory, there are three methods for reading a program:

- Reading automatically when the power is turned ON.
- Reading with the [IC CARD PROGRAM MANAGER] of the NPST−GR.
- Reading with the **F14 (PGRD)** instruction.

Types of IC memory card

There are of two types of IC memory cards, the SRAM type, and a FLASH−EEPROM type. Selection can be made depending on the availability of use.

Type	Memory capacity	Order number
SRAM type	1MB	AIC31000
FLASH−EEPROM type	1MB	AIC30010

SRAM type IC memory card

Most suitable for use with data memory area expansion

When used as expansion memory, use the **F13 (ICWT)**/**P13 (PICWT)** and **F12 (ICRD)**/**P12 (PICRD)** instructions for freely occurring data reading and data writing as desired.

Equipped with a battery used for data backup.

☞ next page

FLASH−EEPROM type IC memory card

Since a backup battery is not necessary it is suited to saving programs.

Perform the program writing with in the [IC CARD MANAGER] of NPST−GR.

When used as expansion memory, it is limited to reading.

Handling the IC memory card

- Avoid high temperature, high humidity and direct sunlight.
- Refrain from jolting or exposing the card to rough handling.
- Do not allow the card to get wet.
- Do not touch or allow foreign objects to contact the connectors.
- Do not place in or near flames.

6.2 Configuration of IC Memory Card

6.2.1 Program Memory and Expansion Memory Areas

The area where the program is saved as is, referred to as the "**program area**" and the area used for expansion of data memory is called the "**expansion memory area**." It is necessary to segregate the areas according to IC memory card use.
Left over capacity in IC memory card cannot be used.

Exclusive use as program memory
When using exclusively for saving programs, it is necessary to use the NPST−GR to designate the whole IC memory card as program memory area.

SRAM type IC memory card:
Format all of the areas of the IC memory card using the [FORMAT IC CARD (SRAM)] of the [IC CARD PROGRAM MANAGER] menu. Refer to the section 6.2.2 for formatting procedure.

FLASH−EEPROM type IC memory card:

Procedure:

1. **Erase all of the areas of IC memory card using [ERASE IC CARD(F&SCRAM)] of the [IC CARD PROGRAM MANAGER]. (* section 6.2.3)**
2. **Use [COPY FILES TO IC CARD (F−EEPROM)] to copy the program from floppy or a hard disk to the IC memory card.**

☞ **Note**

When copying for a second time, re−execute from procedure 1.

Exclusive use as data memory area

When using exclusively for expanding memory, it is necessary to designate the whole IC memory card as “expansion memory area” using NPST−GR.

SRAM type IC memory card

Erase all of the areas using [ERASE IC CARD(F&SRAM)] of the [IC CARD PROGRAM MANAGER] menu. (* section 6.2.3).

Do not format. Data can not be written if formatted.

When an IC memory card has been formatted once, to designate its entire area as “expansion memory area”, select the [ERASE IC CARD (F&SRAM)] option from the [IC CARD PROGRAM MANAGER] menu of the NPST−GR.

Using program memory area and expansion memory area separately

You can set the area to be formatted as desired. All the area other than that formatted area (for program memory area) becomes expansion memory area.

SRAM type

Specify the necessary area for program memory and format with the [FORMAT IC CARD (SRAM)] menu.

```
THE IC MEMORY CARD WILL BE FORMATTED. MEMORY AREA  256KB

    MS-DOS FORMAT AREA [  64]KB      (64KB -256KB)
    EXPANDED MEMORY AREA  98KWORD

* TO CHANGE MS-DOS FORMAT AREA, USE RIGHT OR LEFT KEY.
* EXPANDED MEMORY AREA = ENTIRE MEMORY - MS-DOS FORMAT AREA
* CONTENTS IN IC CARD WILL BE LOST BY FORMATTING
```

☞ **Note**

Record the addresses and store in a safe place.

6.2.2 IC Memory Card Formatting Procedures

SRAM type IC memory card

Before saving the program, first format a IC memory card for MS−DOS and ensure that there is a program memory area for saving the program.

Procedure:

1. **Select the [FORMAT IC CARD (SRAM)] option from the [IC CARD PROGRAM MANAGER] menu of the NPST−GR software.**
2. **When the following screen appears, set the format size (format area).**

```
THE IC MEMORY CARD WILL BE FORMATTED. MEMORY AREA  256KB

    MS-DOS FORMAT AREA [  64]KB      (64KB -256KB)
    EXPANDED MEMORY AREA  98KWORD

* TO CHANGE MS-DOS FORMAT AREA, USE RIGHT OR LEFT KEY.
* EXPANDED MEMORY AREA = ENTIRE MEMORY - MS-DOS FORMAT AREA
* CONTENTS IN IC CARD WILL BE LOST BY FORMATTING
```

3. **Press the <F1> key to execute.**

FLASH−EEPROM type IC memory card

When you copy the program on the disk to the IC memory card, it simultaneously formats the card.

Procedure:

1. **Select the [COPY FILES TO IC CARD (F−EEPROM)] option for the FLASH−EEPROM in the [IC CARD PROGRAM MANAGER] menu of the NPST−GR software.**
2. **When the following screen appears, set the format size (format area) and press the <F1> key.**

```
THE IC MEMORY CARD WILL BE FORMATTED. MEMORY AREA  512KB

    MS-DOS FORMAT AREA [  256]KB      (64KB -512KB)
    EXPANDED MEMORY AREA  128KWORD

* TO CHANGE MS-DOS FORMAT AREA, USE RIGHT OR LEFT KEY.
* EXPANDED MEMORY AREA = ENTIRE MEMORY - MS-DOS FORMAT AREA
* CONTENTS IN IC CARD WILL BE LOST BY FORMATTING
```

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3. When the IC memory card status is displayed, press the <Y> key to format and simultaneously copy the file.

```
[IC CARD FORMAT STATUS]

    IC CARD    : FLASH                                  FLASH
    MEMORY AREA: 512KB
                                          MS-DOS       ( 256KB)   512KB
    MS-DOS AREA: 256KB
    EXPAND AREA: 128KW                 0h
                                          EXPAND AREA  ( 128KW)
                                       7fh

[ESC]: RETURN TO THE PREVIOUS SCREEN.
```

6.2.3 Procedure to Erase IC Memory Card

For the SRAM and FLASH−EEPROM type IC memory cards, before you can use an IC memory card for the expansion memory, you must first erase the IC memory card and secure an expansion memory area.

Procedure:

1. Select the [ERASE IC CARD (F & SRAM)] option in the [IC CARD PROGRAM MANAGER] menu of the NPST−GR software.

2. When the following screen appears, press the <F1> key to erase.

```
[ ERASE ]
< CONTENTS IN IC CARD WILL BE LOST >
F1  :EXECUTE
```

6.2.4 Data Storage Capacity of IC Memory Card

When storing a program or data in the IC memory card, the data storage capacity is as follows.

Program only

Total number of bytes: program file (*.SPG), annotation comment (*.NCB), line space comment (*.GYO), and FAT area (see note)

Keep the total number of bytes for the files given above less than the MS−DOS format capacity.

☞ **Note**

FAT area:
256kB format = 6kB
512kB format = 6.5kB
1M format = 10kB

Program and I/O comment

Total number of bytes: program file (*.SPG), annotation comment (*.NCB), line space comment (*.GYO), I/O comment (*.SCM) and FAT area

Keep the total number of bytes for the files given above less than the MS−DOS format capacity. The I/O comment changes according to the size of the statements.

6.2.5 Managing IC Memory Card

With the NPST−GR software Ver. 3 or later, there is a menu for managing the IC memory card.

```
[IC CARD PROGRAM MANAGER]

[1. LOAD PROG FROM IC CARD (F&SRAM)]
[2. LOAD PROGRAM TO IC CARD (SRAM)]
[3. COPY FILES FROM IC CARD (F&SRAM)]
[4. COPY FILES TO IC CARD (SRAM)]
[5. COPY FILES TO IC CARD (F-EEPROM)]
[6. DELETE FILES (SRAM)]
[7. RENAME A FILE (SRAM)]
[8. CHANGE FILE ATTRIBUTE (SRAM)]
[9. ERASE IC CARD (F&SRAM)]
[A. FORMAT IC CARD (SRAM)]
```

Reading the programs and data stored in the IC memory card (For both the SRAM and FLASH−EEPROM types)

- **[1. LOAD PROG FROM IC CARD (F & SRAM)]:**

  Selects one of the programs stored on the IC memory card and reads its to the NPST−GR.

- **[3. COPY FILES FROM IC CARD (F & SRAM)]:**

  Reads the stored files of program or data from the IC memory card and copies it to a floppy disk or (to the hard disk).

To create a copy of the IC memory card, first copy the files of the IC memory onto a disk, then replace the card with a new IC memory card and copy the files from the disk to the new IC memory card using the [COPY FILES TO IC CARD] option.

Initializing an IC memory card (For both the SRAM and FLASH−EEPROM types)

- **[9. ERASE IC CARD (F & SRAM)]:**

  Clears the entire contents of the IC memory card. Clears all program areas formatted with [A. FORMAT IC CARD (SRAM)], and makes the whole area for expansion memory.

Management of SRAM type IC memory card

- **Before use, [A. FORMAT IC CARD (SRAM)]:**

  MS−DOS formats the IC memory card, and reserves a program memory area for saving the program. Any area not reserved as program memory area becomes expanded memory area.

- **Writing to the IC memory card,**

  [2. LOAD PROGRAM TO IC CARD (SRAM)]:

  Writes the program on the NPST−GR to the IC memory card.

  [4. COPY FILES TO IC CARD (SRAM)]:

  Copies the contents of a floppy disk or hard disk to the IC memory card. Also, with this function, you can select multiple programs and write them to the IC memory card at one time.

- **Other file management functions**

  [6. DELETE FILES (SRAM)]:

  Deletes programs on the IC memory card. Also, with this function, you can select multiple programs and delete at one time.

  [7. RENAME A FILE (SRAM)]:

  Changes the file names and titles of the program on the IC memory card

  [8. CHANGE FILE ATTRIBUTE (SRAM)]:

  Exclusively reads the programs on the IC memory card to read−only files or hidden files.

Writing to FLASH−EEPROM type IC memory card

- **[5. COPY FILES TO IC CARD (F−EEPROM)]:**

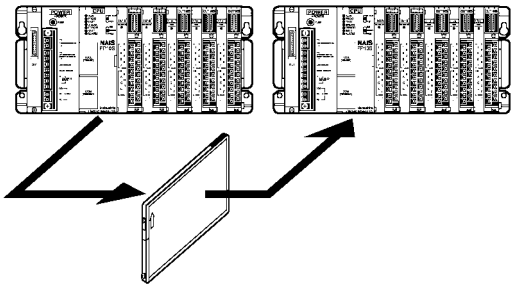
  Writing to the FLASH−EEPROM type IC memory card is done by copying the entire contents of a floppy disk or hard disk at one time.

  With the FLASH−EEPROM type IC memory card, partial editing of contents, file name changes, and erasing cannot be performed. Changes should be made on a disk and then the entire disk should be copied to the IC memory card.

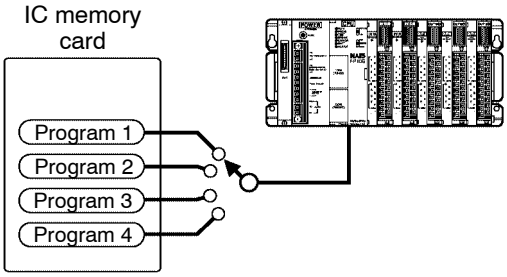
6.3 How To Use IC Memory Card

6.3.1 For Use as Program Memory

By saving the program to a IC memory card, it is simple to create a backup or load it to another CPU.



Furthermore, by saving more than one program, switching between the programs can be done as necessary.



6.3.1.1 Writing the Program

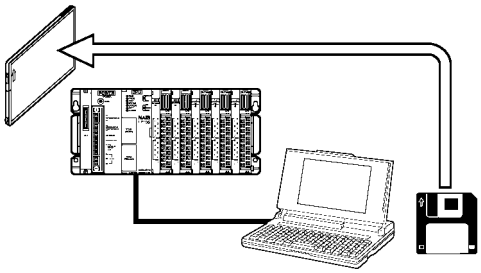
There are 3 methods for writing programs to the IC memory card.

- Use the [IC CARD PROGRAM MANAGER] menu in the NPST−GR software, directly write the program that is saved on the disk to the IC memory card. Possible with all types of IC memory card.
- Directly write the program that is made by the NPST−GR software to the IC memory card. Only possible with the SRAM type IC memory card.
- Write the program on the RAM of the CPU into the IC memory card. Only possible with SRAM type IC memory card.

When writing programs to FLASH−EEPROM type IC memory card, first save the program to disk, then using the [IC CARD PROGRAM MANAGER] option of the NPST−GR software, write to the IC memory card.

☞ next page

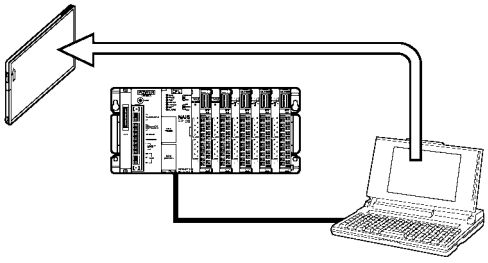
Method 1: Use the [IC CARD PROGRAM MANAGER] function in the NPST−GR software, directly write the program that is saved on the disk to the IC memory card. (For all types of IC memory card)



Procedure:

1. **Select the [SAVE A PROGRAM TO DISK] option in the [PROGRAM MANAGER] menu of the NPST−GR, or the [COPY FILES FROM IC CARD (F & SRAM)] option in the [IC CARD PROGRAM MANAGER] menu, and save the program to floppy disk or hard disk.**
2. **From the [IC CARD PROGRAM MANAGER] menu of the NPST−GR, select the [COPY FILE TO IC CARD] option of the IC memory card type that is to be used.**
3. **Press the <F1> key to execute.**
   - **You can select more than one file and copy them at one time.**
   - **If you need the contents to be copied to the built−in RAM, when the power is turned ON, change the name of the program to AUTOEXEC. (* section 6.3.1.2)**

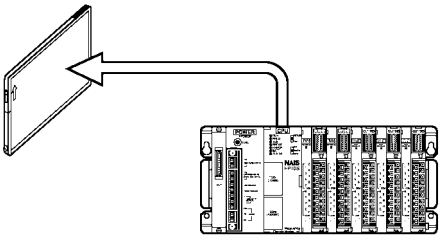
Method 2: Directly write the program that is made by the NPST−GR software to the IC memory card. (For the SRAM type IC memory card)



Procedure:

1. **Select the [LOAD PROGRAM TO IC CARD (SRAM)] option in the [IC CARD PROGRAM MANAGER] menu of the NPST−GR software.**
2. **Press the <F1> key to execute.**

Method 3: Write a program on the RAM of the CPU into the IC memory card. (For the SRAM type IC memory card)



By performing the following procedures, the data on the RAM of the CPU is written to the IC memory card and named “AUTOEXEC.SPG”.

Procedure:

1. **Press the <CTRL> and <ESC> keys together to change to the online monitor mode.**
2. **Press the <ESC> key to display the [NPST MENU]. Select the [COPY PROGRAM BETWEEN ROM & RAM] option of the [PROGRAM MANAGER] and then press the <ENTER> key.**
3. **Press the <F2> key to change the [LOAD COPY RAM TO ROM].**
4. **Press the <F1> key to execute.**

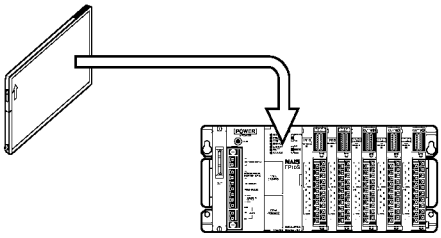
6.3.1.2 Reading the Program

There are 4 methods of reading the program saved in the IC memory card.

- Read the program on the IC memory card and directly load it into the built–in RAM of the CPU when the power is turned ON.
- Use the programming tool to read the program of the IC memory card and directly load it into the built–in RAM of the CPU.
- Use the [LOAD PROGRAM FROM IC CARD] option in the [IC CARD PROGRAM MANAGER] menu of the NPST–GR, and select one of the programs saved in the IC memory card and read it to the NPST–GR (memory of personal computer).
- Use the **F14 (PGRD)** instruction to read the program from the IC memory card, and directly load it into the built–in RAM of the CPU.

☞ next page

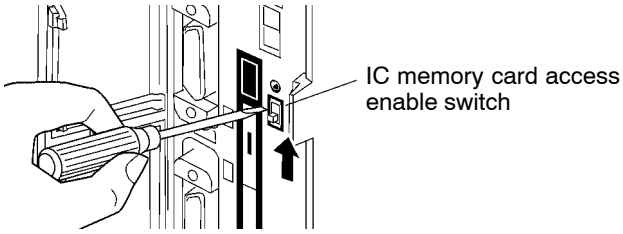
Method 1: Read the program on the IC memory card and directly load it into the built–in RAM of the CPU when the power is turned ON.
By just turning ON the CPU, the device automatically reads the program of the IC memory card and loads the program to the built–in RAM of the CPU.



The program that is automatically read is the program named “AUTOEXEC” and is the target of automatic reading.

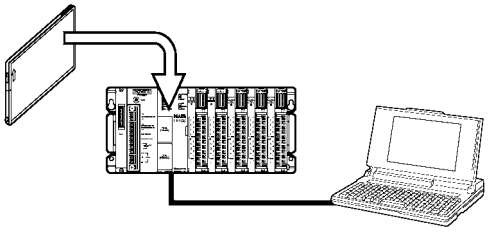
Procedure:

1. **While the power is turned OFF, set the program memory selection (SW5) of the operation condition switches on the CPU to the ON (using optional memory) position, and set the IC memory card access enable switch to ON position.**



2. **Turn ON the CPU.**

Method 2: Use the programming tool to read the program of the IC memory card and directly load it into the built–in RAM of the CPU.
With simple operation of the programming tool, reads the program saved on the IC memory card, and load it to the built–in RAM of the CPU.



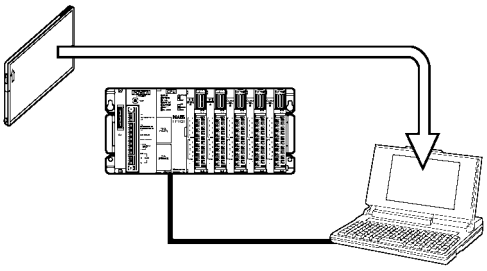
The program read is the program named “AUTOEXEC.SPG”.

☞ next page

Procedure:

1. **Press the <CTRL> and <ESC> keys together to change to the online monitor mode.**
2. **Press the <ESC> key to display the [NPST MENU]. Select the [COPY PROGRAM BETWEEN ROM & RAM] option of [PROGRAM MANAGER] menu and then press the <ENTER> key.**
3. **Press the <F2> key to change the [COPY ROM TO RAM] option.**
4. **Press the <F1> key to execute.**

Method 3: Use the [LOAD PROGRAM FROM IC CARD] option in the [IC CARD PROGRAM MANAGER] menu of the NPST−GR, and select one of the programs saved in the IC memory card and read it to the NPST−GR (memory of personal computer).

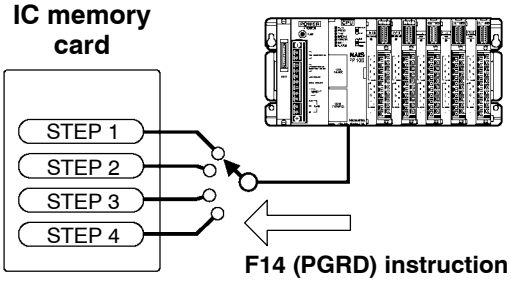


Procedure:

1. **Select the [LOAD PROGRAM FROM IC CARD] option in the [IC CARD PROGRAM MANAGER] menu of the NPST−GR software.**
2. **Select the desired file from the displayed file names.**
3. **Press the <F1> key to load the program.**

When loading the program on the NPST−GR to the built−in RAM of the CPU, select the [LOAD A PROGRAM TO PLC] option of the [PROGRAM MANAGER] menu.

Method 4: Use the **F14 (PGRD)** instruction to read the program from the IC memory card and directly load it into the built–in RAM of the CPU.



By first saving the programs you desire on the IC memory card, you can use the **F14 (PGRD)** instruction in the program, to switch a program while in the RUN mode (while in operation).

The following details the describe the program after executing **F14 (PGRD)** instruction.

- The program will continue executing until the **END** instruction is executed.
- The CPU enters the PROG. mode and the program is read from the IC memory card and load to the built–in RAM of the CPU.
- The CPU automatically switches to the RUN mode, and the new program executes.

Program Example

With **F14 (PGRD)** instruction, specify a saved file name by the NPST–GR to call up the program of from IC memory card.

```
─┤ ├─[F14  PGRD, DT  100          ]
                   └── "STEP1"
```

For the program above, the contents ("STEP 1") stored in DT100 is the file name used to call up the program.

To store the program name to registers such as DT100, you can write it with alphanumeric code using **F0 (MV)** or **F1 (DMV)** instruction, or you can write it with ASCII conversion using **F95 (ASC)** instruction. For more details, refer to the programming manual.

☞ **Note**

There are dangers involved when switching programs while in the RUN mode. Carefully read the section regarding the F14 (PGRD) instruction in the programming manual.

6.3.2 For Use as Expansion Memory

6.3.2.1 Outline of Expansion Memory

The expansion memory area is an independent area from the internal memory of the CPU that stores word data. Use the **F12 (ICRD)** and **F13 (ICWT)** instructions to read and write data to this area. Below are some of the things that you can do by using the expansion memory area.

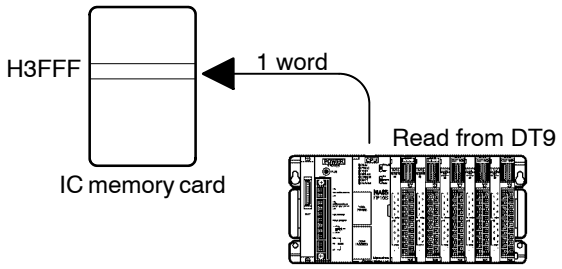
As reading and writing is easily done using high–level instructions, you can to use the expansion memory as external memory for the CPU.

Writing

Use the **F13 (ICWT)** instruction to load the word data stored in the data register of the CPU to the IC memory card.

```
─┤ ├─[F0  MV, K  100, DT 9          ]
   [F13  ICWT, DT  9, K 1, H3FFF     ]
```

With the above program, after the constant K100 is stored in DT9, **F13 (ICWT)** instruction is used to write one word of data from the beginning of DT9 (K100) to the H3FFF address of the IC memory card. For details refer to the **F13 (ICWT)** instruction of the programming manual.



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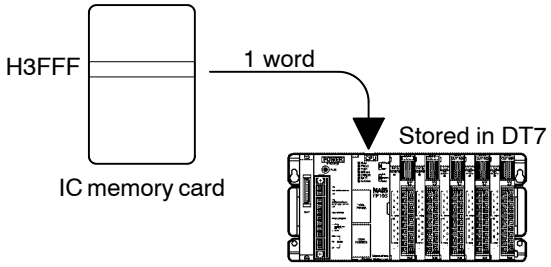
Reading

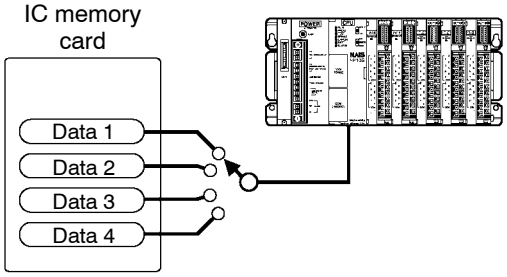
Use the **F12 (ICRD)** instruction to load the word data stored on the IC memory card to the data register of the CPU.

```
─┤ ├─[F12  ICRD, H3FFF, K 1, DT 7        ]
```

The above program reads a one word data from the H3FFF address of the IC memory card to DT7. For details refer to the **F12 (ICRD)** instruction of the programming manual.



When dealing with many different data or other such applications, you can create a table to store the different control data and easily switch between the data according to the data type you are using.



Create a data table in the IC memory card, such as outlined above, so that the data is read to the CPU every time you switch data.

6.3.2.2 Configuration of Expansion Memory Area

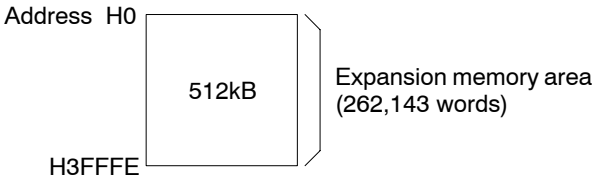
Areas of the IC memory card that are not formatted can be used as expansion memory area.

One word (two bytes) can be stored in one address. As the following example illustrates, in a 512kB area, data of 262,143 words can be stored.

$$\frac{(512 \times 1024)\ \text{bytes}}{2} = 262{,}143\ \text{words}$$

In the expansion memory area, the addresses are numbered by word units and, regardless of the size of the formatted area, the starting address is numbered as 0 (H0). For example, the addresses for a 512kB (256 k words) area are from as H0 to H3FFFE.

Example: When a 512kB of SRAM type IC memory card is designated as expansion memory (unformatted).



Chapter 7

Self−Diagnostic and Troubleshooting

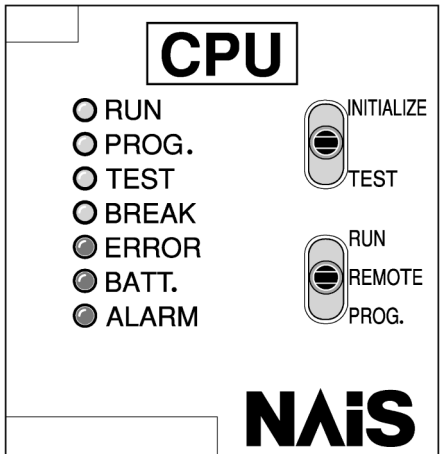
7.1 Self−Diagnostic Function

7.1.1 Status Indicator LEDs on CPU

Condition	LED status							Description	Program execution status
	RUN	PROG.	TEST	BREAK	ERROR	BATT.	ALARM		
Normal condition	ON	OFF	OFF	OFF	OFF	OFF	OFF	Normal operation in RUN mode	Operation
	OFF	ON	Varies	OFF	OFF	OFF	OFF	Normal operation in PROG. mode	Stop
	Flashes	OFF	Varies	OFF	OFF	OFF	OFF	Forcing ON/OFF in RUN mode	Operation
	OFF	ON	ON	Varies	Varies	OFF	OFF	TEST/RUN mode (break condition)	Stop
	ON	OFF	ON	OFF	Varies	OFF	OFF	TEST/RUN mode (operating condition)	Operation
Abnormal condition	OFF	Varies	Varies	Varies	ON	Varies	OFF	When a self-diagnostic error occurs (stops)	Stop
	ON	OFF	OFF	OFF	ON	Varies	OFF	When a self-diagnostic error occurs (continues)	Operation
	Varies	Varies	Varies	Varies	Varies	ON	OFF	Backup battery error occurs	Operation
	Varies	Varies	Varies	Varies	Varies	Varies	ON	When a watchdog timer error occurs	Stop
	OFF	Flashes	Varies	OFF	Varies	Varies	OFF	MEWNET-F slave station waiting error occurs	Stop

The FP3/FP10SH CPU has a self-diagnostic function which identifies errors and stops operation if necessary.

When an error occurs, the status of the status indicator LEDs on the CPU vary, as shown in the table above.



7.1.2 Operation When an Error Occurs

Normally, if an error occurs, operation of the FP3/FP10SH stops.

There are some instances in which operation continues even if an error occurs, such as with a battery error.

The user may select whether operation is to be continued or stopped if a duplicate output error or operation error occurs, by setting the system registers. You can set the system registers with NPST−GR software.

Procedure:

1. **Press the <ESC> key to display the [NPST MENU], select the [SYSTEM REGISTER] option from the [PLC CONFIGURATION] menu and press <ENTER> key.**
2. **In the [PLC CONFIGURATION] screen, press the <F8> key and select the [ACT ON ERROR] option.**

Register No.	Item	Descriotion
20	DUPLICATE OUTPUT	[DISE, ENAB]
21	OUTPUT UNIT FUSE BLOW	[STOP, CONT]
22	INTELLIGENT UNIT ERROR	[STOP, CONT]
23	I/O VERIFY ERROR	[STOP, CONT]
24	W.D.T TIME OUT BY OPE JAM	[STOP, CONT]
25	UNUSED	
26	OPERATION ERROR	[STOP, CONT]
27	REMOTE I/O SLAVE LINK ERROR	[STOP, CONT]
28	I/O ERROR IN REMOTE I/O SLAVE	[STOP, CONT]
29	UNUSED	
4	BATTERY ERROR INDICATION	[ENAB, DISA]

7.1.2.1 Allowing Duplicated Output

When you change system register 20 settings (“ENAB”) using the NPST−GR software, duplicated output is not regarded as an error and the FP3/FP10SH continuse to operate.

7.1.2.2 Continuing After An Operation Error

When you change system register 26 settings (“CONT”) using the NPST−GR software, the FP3/FP10SH continues to operate. In this case, even if the FP3/FP10SH continues to operate, this is regarded as an error.

This applies to system registers 21 through 28 as well.

7.2 Troublesooting

7.2.1 If the ERROR LED Lights

<Condition>

The self−diagnostic error occurs.

<Procedure 1>

Replace the backup battery of the CPU when the BATT. LED is ON. (* section 8.1.1.2)

<Procedure 2>

Check the error code using the programming tool.

Using NPST-GR software

In the ONLINE mode, select “STATUS DISPLAY.” At the bottom of the “STATUS DISPLAY” window, you can find the error code.

SLF DIAGN ERR CD (45) [OPERATION ERROR]

Error code Comments

Using FP programmer II Ver.2

Press the keys on the FP programmer II Ver.2 as shown on the right.
When self-diagnostic error occurs, the screen shown on the right is displayed.

OP− 110
FUNCTION ERR E45

Error code is 1 to 9

<Condition>

There is a syntax error in the program.

<Procedure 1>

Change to PROG. mode and clear the error.

<Procedure 2>

Execute a total−check function to determine the location of the syntax error.

Refer to NPST−GR software manual for details about the total−check method.

☞ next page

Error code is 20 or higher

<Condition>

A self−diagnostic error other than a syntax error has occurred.

<Procedure 1>

Use the programming tool in PROG. mode to clear the error.

Using NPST-GR software

Press the **<F3>** key in the “STATUS DISPLAY” menu described on the previous page. Error code 43 and higher can be cleared.

Using FP programmer II Ver.2

Press the keys as follows. Error code 43 and higher can be cleared.

ACLR (−) OP 1 1 2 ENT SHIFT SC (DELT) INST

In the PROG. mode, the power supply can be turned OFF and then ON again to clear the error, but all of the contents of the operation memory except hold type data are cleared.
An error can also be cleared by executing a self−diagnostic error set instruction **F148 (ERR)**/**P148 (PERR)**.

For version 4.3 or earlier FP3 CPU, change to the PROG. mode and turn the power OFF and ON to clear the error condition.

<Procedure 2>

Follow the procedures described in the table of error codes (* section Appendix F).

☞ **Note**

When an operation error (error code 45) occurs, the address at which the error occurred is stored in special data registers (FP3: DT9017 and DT9018, FP10SH: DT90017 and DT90018). If this happens, monitor the address at which the error occurred before cancelling the error.

7.2.2 If the ALARM LED Lights

<Condition>

The system watchdog timer has been activated and the operation of FP3/FP10SH has been stopped.

↓

<Procedure 1>

Set the mode selector of the FP3/FP10SH CPU from RUN to PROG. and turn the power OFF and then ON.

↓

- If the ALARM LED is turned ON again, there is probably an abnormality in the FP3/FP10SH. Please contact your dealer.
- If the ERROR LED is turned ON, go to section 7.2.1.

<Procedure 2>

Set the mode selector from PROG. to RUN.

If the ALARM LED is turned ON, the program execution time is too long. Check the program, referring the following:

- Check if instructions such as **JP** or **LOOP** are programmed in such a way that a scan can never finish.
- Check that interrupt instructions are executed in succession.

7.2.3 If the LED (POWER) of Power Supply Unit Does Not Light

<Procedure 1>

Check wiring of power supply unit.

↓

<Procedure 2>

For power supply unit (AFP3631 or AFP3638), check that the voltage selecting terminal is set correctly (* section 2.6).

↓

For use at 100 to 120 V AC, short the voltage selecting terminals with the short circuiting bar.

☞ next page

<Procedure 3>

Check if the power supplied to the power supply unit is in the range of the rating (* section 2.6.1).

- If the capacity of internally supplied power (5 V) is insufficient, investigate different unit combinations.
- If the capacity of externally supplied power (24 V) is insufficient, install a separate 24 V DC power supply.

<Procedure 4>

Check if a fuse has blown.

If a fuse has blown, replace the fuse (* section 8.1.3).

<Procedure 5>

Disconnect the power supply wiring to the other devices if the power supplied to the power supply unit is shared with them.

If the LED on the power supply unit turn ON at this moment, pepare another power supply for other devices or increase the capacity of the power supply.

7.2.4 If Outputting Does Not Occur as Desired

Proceed from the check of the output side to the check of the input side.

Check of output condition <1>
Output indicator LEDs are ON

<Procedure 1>

Check the wiring of the loads.

<Procedure 2>

Check if the power is properly supplied to the loads.

- If the power is properly supplied to the load, there is probably an abnormality in the load. Check the load again.
- If the power is not supplied to the load, there is probably an abnormality in the FP3/FP10SH's output circuit. Please contact your dealer.

☞ next page

Check of output condition <2>

Output indicator LEDs are OFF

<Procedure 1>

Monitor the output condition using a programming tool.

– If the output monitored is turned ON, there is probably a duplicated output error.

<Procedure 2>

Forcing ON the output using forcing I/O function.

– If the output indicator LED is turned ON, go to input condition check.

– If the output indicator LED remains OFF, there is probably an abnormality in the output unit. Please contact your dealer.

Check of input condition <1>

Input indicator LEDs are OFF

<Procedure 1>

Check the wiring of the input devices.

<Procedure 2>

Check that the power is properly supplied to the input terminals.

– If the power is properly supplied to the input terminal, there is probably an abnormality in the input unit. Please contact your dealer.

– If the power is not properly supplied to the input terminal, there is probably an abnormality in the input device or input power supply. Check the input device and input power supply.

Check of input condition <2>

Input indicator LEDs are ON

<Procedure>

Monitor the input condition using a programming tool.

– If the input monitored is OFF, there is probably an abnormality with the input unit. Please contact your dealer.

– If the input monitored is ON, check the program again.
Also, check the leakage current at the input devices (e.g., two–wire type sensor) and check the program again referring the following:
Check for the duplicated use of output. Check the program flow when a control instruction such as **MC** or **JP** is used.
Check the settings of the I/O allocation.

7.2.5 If a Communication Error Appears When Using NPST−GR

<Procedure 1>

Check if the baud rate and data length settings of the FP3/FP10SH and NPST−GR are the same.

NPST-GR baud rate setting

1. Open [NPST MENU] by pressing the **<ESC>** key, then select “NPST CONFIGURATION” to skip to the [NPST CONFIGURATION] subwindow.
2. Select a baud rate (9600 or 19200).
3. Press the **<F1>** key and select “SAVE DISK? YES” to register this change onto the disk.

FP3/FP10SH baud rate setting

Use the baud rate selector to enter the setting for the FP3/FP10SH. (* section 5.2.1)

☞ **Note**

Depending on the personal computer, there are times when baud rate of 19,200 bps or greater are not supported. If problems occur, set both the personal computer and FP3/FP10SH to 9,600 bps.

<Procedure 2>

Check the FP PC cable and RS232C adapter.

RS232C adapter needs to be customized to match your computer.

<Procedure 3>

Confirm the setting of the personal computer referring to the manual for your computer.

Set your personal computer’s RS232C parameter to asynchronous.

7.2.6 If a Protect Error Message Appears

When ROM is installed in the FP3/FP10SH CPU

If the ROM is installed on the FP3/FP10SH CPU, the program cannot be modified and a “protect error” occurs.

<Procedure 1>

Turn OFF the power of the FP3/FP10SH and set the memory selector of CPU to the RAM position.

↓

<Procedure 2>

Modify the program of the internal RAM using the programming tool.

↓

<Procedure 3>

Save the modified program to the memory or master memory (* section 5.4.4) and start operation again.

If the program memory is protected

<Procedure>

Set the program memory protection switch of the operation condition switches for CPU to OFF (write enabled) position.

When a password is set for the FP3/FP10SH

<Procedure>

Enter a password in the [SET PLC PASSWORD] menu in NPST−GR software and select “enable.”

1. Open [NPST MENU] by pressing the **<ESC>** key, and then select “PLC CONFIGRATION” to skip to the [PLC CONFIGRATION] window. In the [PLC CONFIGRATION] window, select “SET PLC PASSWORD.”
2. Enter the password and select enable (ENAB).

Chapter 8

Maintenance

8.1 Replacement of Spare Parts

8.1.1 Replacement of Backup Battery

8.1.1.1 Lifetime of Backup Battery

The battery lifetime may vary depending on type of CPU you use.

CPU type			Battery lifetime (at 25 °C/77 °F) (Typical lifetime in actual use)
FP3	AFP3210C–F		17,000 hours or more (approx. 34,000 hours)
	AFP3211C–F, AFP3220C–F		10,000 hours or more (approx. 22,000 hours)
FP10SH	AFP6211V3	CPU only	9,500 hours or more (approx. 57,000 hours)
		When used expansion memory	7,600 hours or more (approx. 44,000 hours)
	AFP6221V3	CPU only	4,800 hours or more (approx. 29,000 hours)
		When used expansion memory	4,300 hours or more (approx. 25,000 hours)

The backup battery should be replaced periodically, to avoid overlooking a weakened battery.

A drop in the battery voltage can be confirmed with special internal relays R9005 and R9006, the ERROR LED and BATT. LED. Although the backup battery function does not stop operation, be sure to replace new battery within a week.

Backup battery
Order number of backup battery with connector for FP3/FP10SH: AFP8801

☞ **Note**

Never throw batteries into a fire, disassemble or charge the battery in order to prevent accidents such as bursting, fire or heat generation.

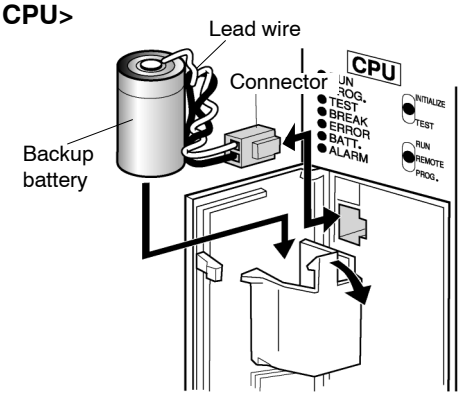
8.1.1.2 Replacement Method of Battery

When replacing the battery, be sure to keep power of CPU ON.
If the battery is to be replaced with the power OFF, apply power to the FP3/FP10SH CPU for at least 30 minutes, and then turn the power supply OFF and replace it within 10 minutes.

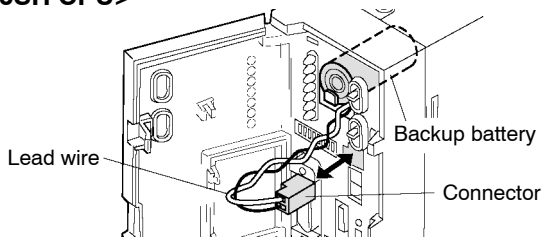
Procedure:

1. **Open the unit cover of CPU.**
2. **Pull the lead wire to remove the connector.**

<FP3 CPU>



<FP10SH CPU>



3. **Insert the new battery and connect the connector.**
4. **Close the unit cover making sure that lead wire is not caught in the cover.**
5. **To cancel the error condition, perform either the following operations:**
   - **Turn the INITIALIZE/TEST switch ON.**
   - **Turn the power OFF and then back ON.**

☞ next page

☞ **Note**

Be aware that if you turn ON the initialize/test switch, the data register of hold type and other contents of operation memory will also be initialized. (For the FP10SH, by using the system register, you can set it so that it does not clear the operation memory. For more details, refer to the system register on programming manual.)

8.1.2 Battery of IC Memory Card

8.1.2.1 Battery Lifetime

Type	Order number	Memory capacity	Battery lifetime
SRAM type IC memory card	**AIC31000**	**1 MB**	2 years or more

The battery should be replaced periodically, to avoid overlooking a weakened battery.

A drop in the battery voltage can be confirmed with the error code K54 or K55 in special data register DT90000 and the ERROR LED turns ON. The error codes can be confirmed with the programming tool (NPST-GR software).

- Error code K54: Data in the IC memory card cannot guaranteed. Replace the battery of the IC memory card as soon as possible.
- Error code K55: Data in the IC memory card is maintained but the voltage of the battery for IC memory card lowers. Replace the battery of the IC memory card.

Although the backup battery function does not stop operation, be sure to replace new battery within a week.

For the FP10SH, the battery condition of the IC memory card can be judged using the special internal relays R9101 and R9102.

R9101	R9102	Battery condition of IC memory card
OFF	**OFF**	No battery replacement required.
OFF	**ON**	Battery replacement is necessary. The data in the IC memory card is maintained.
ON	**OFF**	Battery replacement is necessary. The data in the IC memory card cannot guaranteed.
ON	**ON**	

Backup battery for IC memory card

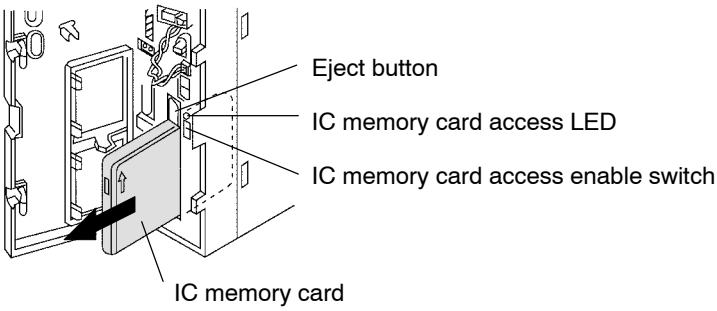
Type	Description
SRAM type IC memory card (AIC31000)	Lithium battery CR2025 or equivalent

8.1.2.2 Replacement Method of Battery

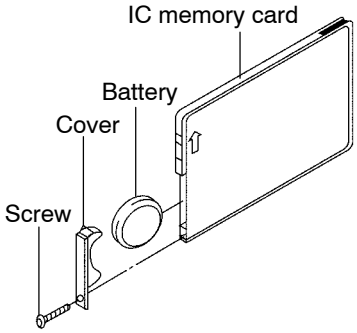
The battery can be replaced while the power supply of FP10SH is turned ON.

Procedure:

1. **Open the unit cover of CPU.**
2. **Set the IC memory card access enable switch to OFF position. The IC memory card access LED turns OFF.**



3. **Pull out the IC memory card.**
4. **Use the screwdriver supplied with the IC memory card to remove the screw on the card side.**



5. **Remove the battery and insert the new battery.**
6. **Attach the cover and tighten the screw in place.**
7. **Insert the IC memory card to the slot for the card in CPU until the eject button sticks out.**
8. **Set the IC memory card access enable switch to ON position.**

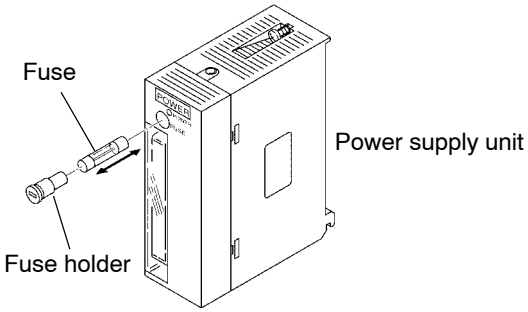
☞ **Note**

If you are replacing the battery after turning OFF the power supply of FP10SH, then steps 2 and 8 are unnecessary. Though be sure to finish the replacement procedure within 10 minutes.

8.1.3 Replacement of Fuse for Power Supply Unit

8.1.3.1 Replacement Method of Fuse

Be sure to turn OFF the power to the FP3 and then replace fuse.



Procedure:

1. **Remove the fuse holder with a flat-head screwdriver.**
2. **Replace the fuse with a new one.**
3. **Attach the fuse holder by pressing it in.**

Replacement fuse for power supply unit
Fuses are for the FP3 power supply unit only. Be sure to specify the appropriate order number given below.

Description	Order number
2A type (FP3 power supply unit: AFP3631, AFP3634)	AFP88021
4A type (FP3 power supply unit: AFP3638)	AFP88022

☞ **Note**

Always have the power supply turned OFF while replacing a fuse.

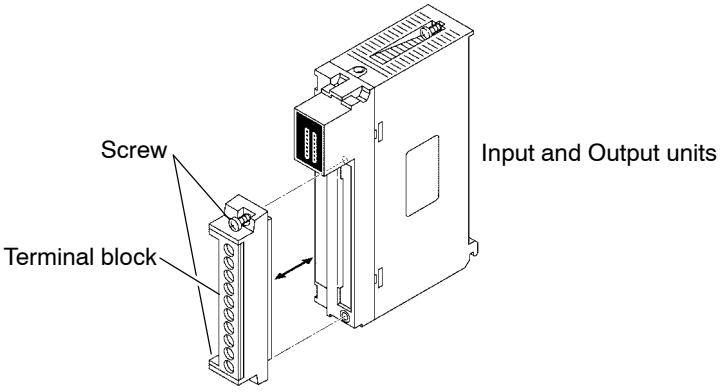
8.1.4 Removable Terminal Block for Input and Output Units

The removable terminal block is used on the terminal type input and output units.

The removable terminal block can be removed while it is still wired. Therefore, if a malfunction or other error occurs, replacement of the unit and other maintenance procedures can be carried out speedily.

Loosen the screws on both ends to remover the terminal block. Then pull out the terminal block from the unit.

Attach the terminal block to the unit, and be sure to tighten the screws well.



8.1.5 Replacement of Relay for Output Unit

8.1.5.1 Replacement Method of Relay

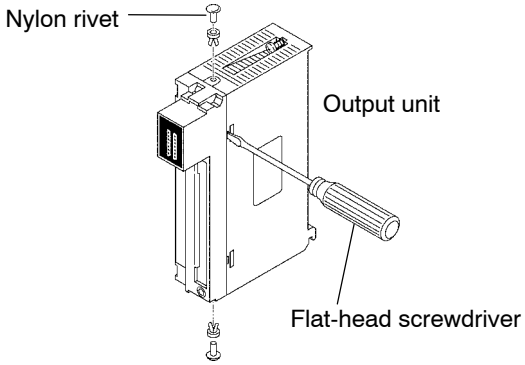
The relay type output unit with relay socket has relay replacement possibility. If the relay fails, you can replace only relay. Be sure to turn OFF the power the FP3 and then remove the output unit from the backplane before replacing relay.

Procedure:

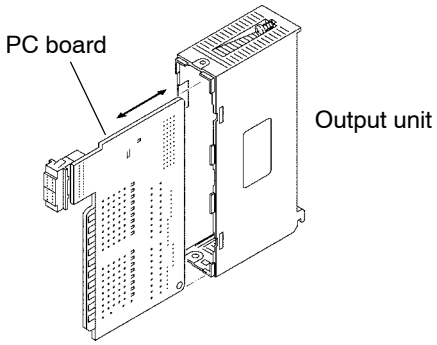
1. **Remove the nylon rivet on the top and bottom of the output unit.**

☞ next page

2. **Insert a flat-head screwdriver into the side slot of the unit and remove the front case by rotating the screwdriver.**



3. **Pull the PC board out of the case.**



4. **Remove the failed relay from the socket and insert a new one.**
5. **Follow the above steps in reverse order to reassemble the unit.**

Replacement relay

Be sure to specify the appropriate order number given below.

Output unit order number	Relay order number
AFP33203–F	APC33125

8.1.6 Replacement of Fuse for Output Unit

Replacement fuse for output unit
Be sure to select the fuse referring to the table below.

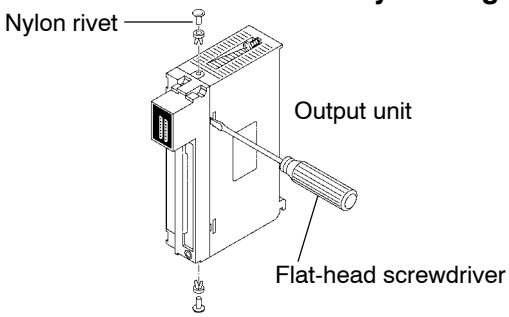
Output unit			Fuse
Type		**Order number**	**Order number**
Transistor output type	**NPN 16 points**	AFP33483−F	AFP88042
	PNP 16 points	AFP33583−F	
Triac output type	**16 points**	AFP33703	AFP88032

8.1.6.1 Replacement Method of Fuse

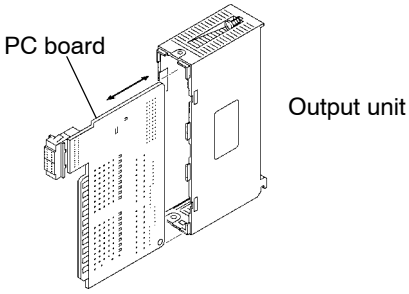
Be sure to turn OFF the power the FP3/FP10SH and then remove the output unit from the backplane before replacing fuses.

Procedure:

1. **Remove the nylon rivet on the top and bottom of the unit.**
2. **Insert a flat-head screwdriver into the side slot of the unit and remove the front case by rotating the screwdriver.**



3. **Pull the PC board out of the case.**



4. **Remove the failed fuse from the holder and insert a new one.**
5. **Follow the above steps in reverse order to reassemble the unit.**

8.2 Preventive Maintenance

Although the FP3/FP10SH system has been designed in such a way to minimize maintenance and offer troublefree operation, several maintenance aspects should be taken into consideration.

If preventive maintenance is performed periodically, you will minimize the possibility of system malfunctions.

Inspection item	Inspection description	Basis of judgement	Reference
Power supply unit	Check POWER LED on power supply unit	Normal if ON	Section 2.6
	Power supply unit	Periodic replacement (approx. 20,000 hours operation)	
CPU display	Check RUN LED	ON in RUN state	Section 2.4, 2.5 and 7.1
	Check ERROR LED	Normal if OFF	
	Check ALARM LED	Normal if OFF	
	Check BATT. LED	Normal if OFF	
Input/output unit display	Check input/output display LED	Normal if ON during ON, and OFF during OFF	Section 2.8
Installation condition	Backplane mounting looseness	Securely mounted	Section 4.1
	Looseness and/or play in unit		
Connection condition	Looseness of terminal screw	No looseness	Section 4.1
	Proximity of connection in pinch terminal	Pinched parallel	
	Connector looseness	Locked in	
	Connection condition of expansion cable	Connector section is not loose	
Power supply voltage of power supply unit	Voltage between terminals	AFP3631 and AFP3638: 85 to 132 V AC or 170 to 264 V AC	Section 4.2
		AFP3634: 16.8 to 28.8 V DC	
Power supply voltage for input/output	Voltage between terminals	Within the specified range of each unit	Section 2.9 to 2.11
Ambient environment	Ambient temperature	0 to 55 °C/32 to 131 °F	Section 4.1
	Ambient humidity	30 to 85 % RH	
	Operating condition	No dust or corrosive gas	
Backup battery	Battey for CPU	Regular replacement	Section 8.1.1
	Battery for IC memory card	Regular replacement	Section 8.1.2
Fuse	Fuse of power supply unit	Regular replacement	Section 8.1.3
	Fuse of output unit	Regular replacement	Section 8.1.6

Appendix A

Performance Specifications

A.1 FP10SH Performance Specifications

Item		Descriptions	
Order number		**AFP6221V3**	**AFP6211V3**
Program method		relay symbol	
Control method		cyclic operation	
Controll–able I/O points	**using one backplane**	max. 512 points	
	using master and three expansion backplanes	max. 2,048 points	
	using remote I/O system	max. 8,192 points	
Program memory	**built-in memory**	RAM	
	Optional memory	IC memory card **(* Note 4)** or EPROM/FROM **(* Note 5)**	
Program capacity		approx. 30 k steps (Approx. 60 k or 120 k steps available by installing optional expansion memory.)	
Number of instruc–tions	**basic**	95 types	
	high-level	431 types	
Operation speed (typical value)	**basic instructions**	from 40 ns per instruction	from 100 ns per instruction
	high–level instructions	from 80 ns per instruction	from 200 ns per instruction
Relays	**external input relays (X)**	8,192 points	
	external output relays (Y) (* Note 1)	8,192 points	
	internal relays (R) (* Note 2)	14,192 points	
	timer/counter (* Note 2)	total 3,072 points (TM number of timer (T) and counter (C) can be changed.) – down type ON-delay timer: 0.001 to 32.767 s, 0.01 to 327.67 s, 0.1 to 3276.7 s or 1 to 32,767 s – down type preset counter: 1 to 32,767 counts	
	link relays (L) (* Note 1, 2)	10,240 points	
	pulse relays (P) (* Note 1, 2)	2,048 points	
	alarm relays (E) (* Note 1, 2)	2,048 points	

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A.1 FP10SH Performance Specifications

Item		Descriptions	
Order number		**AFP6221V3**	**AFP6211V3**
Memory areas	**data registers (DT) (* Note 2)**	10,240 words	
	file registers (FL) (* Note 2)	32,765 words	
	link data registers (LD) (* Note 2, 3)	8,448 words	
	timer/counter set value area (SV)	3,072 words	
	timer/counter elapsed value area (EV)	3,072 words	
	index registers (I)	14 words (I0 to ID) (with bank switching, 224 words portions can be used)	
Differential points (DF and DF/)		unlimited number of points	
Auxiliary timer		unlimited number of points, down type timer (0.01 to 327.67 s)	
Master control relay points (MCR)		256 points (when using the 90 k step expansion memory, up to a total of 512 points can be used for the no. 1 and 2 programs)	
Number of labels (JP and LOOP)		256 points (when using the 90 k step expansion memory, up to a total of 512 points can be used for the no. 1 and 2 programs)	
Number of step ladder (* Note 2)		1,000 steps (can only be used for the no. 1 program)	
Number of subroutine		100 subroutines (can only be used for the no. 1 program)	
Number of interrupt program		25 program (can only be used for the no. 1 program)	
Comment input function		available (either the IC memory card board or ROM operation board are required)	
Sampling trace function		max. 1,000 samples (16 contacts and 3 words/sample)	
Clock/calendar function		year, month, day, hour, minute, second and day of week	
Link functions		PC link, computer link, data transfer, remote programming and MODEM capability	
Self-diagnostic function		watching dog timer, memory malfunction detection, I/O malfunction detection, backup battery malfunction detection, program syntax check, etc.	
Other functions		program edition during RUN, forced ON/OFF, interrupt input, test run and constant scan	
Memory backup time (lithium battery storage time)	**CPU only**	min. 4,800 hours (typical : approx. 29,000 hours)	min. 9,500 hours (typical : approx. 57,000 hours)
	when used expansion memory	min. 4,300 hours **(* Note 6)** (typical : approx. 25,000 hours)	min. 7,600 hours **(* Note 6)** (typical : approx. 44,000 hours)

☞ next page

☞ Notes

- **(*1): Can also be used as an internal relay.**
- **(*2): Hold or non–hold type can be set.**
- **(*3): Can also be used as a data register.**
- **(*4): In addition to the IC memory card, the IC memory card board (AFP6209A) is required.**
- **(*5): In addition to the ROM, the ROM operation board (AFP6208) is required.**
- **(*6): The value when the 90 k steps type expansion memory board (AFP6205) is used.**

A.2 FP3 Performance Specifications

Item		Descriptions		
Order number		**AFP3210C–F**	**AFP3211C–F**	**AFP3220C–F**
Program method		relay symbol		
Control method		cyclic operation		
Controll–able I/O points	**using one backplane**	max. 512 points		
	using master and two expansion backplanes	max. 1,536 points		
	using remote I/O system	max. 2,048 points		
Program memory	**built-in memory**	RAM		
	optional memory	EPROM/EEPROM		
Program capacity (* Note 1)		max. 9,727 steps		max. 15,871 steps
Number of instruc–tions	**basic**	83 types		
	high-level	237 types	241 types	241 types
Operation speed (typical value)	**basic instructions**	from 0.5 μs per instruction		
	high–level instructions	varies from 10 μs to 100 μs		
Relays	**external input relays (X)**	2,048 points		
	external output relays (Y) (* Note 2)	2,048 points		
	internal relays (R) (* Note 3)	1,568 points		
	timer/counter (C) (* Note 3)	total 256 points (The numbers of timer (T) and counter (C) can be changed.) down type ON-delay timer: 0.01 to 327.67 s, 0.1 to 3276.7 s or 1 to 32767 s down type preset counter: 1 to 32,767 counts		
	link relays (L) (* Note 2, 3)	1,024 points × 2 roots (2 PC links)		

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Item		Descriptions		
Order number		**AFP3210C−F**	**AFP3211C−F**	**AFP3220C−F**
Memory areas	**data registers (DT) (* Note 3)**	2,048 words		
	File registers (FL) (* Note 1, 3)	0 to 8,192 words		8,192 to 22,525 words
	link data registers (LD) (* Note 3, 4)	128 words × 2 roots (2 PC links)		
	timer/counter set value area (SV)	256 words		
	timer/counter elapsed value area (EV)	256 words		
	index registers (IX, IY)	2 words		
Differential points (DF and DF/)		unlimited number of points		
Auxiliary timer		unlimited number of points, down type timer (0.01 to 327.67 s)		
Master control relay points (MCR)		64 points		
Number of labels (JP and LOOP)		256 labels		
Number of step ladder (* Note 3)		1,000 stages		
Number of subroutine		100 subroutines		
Number of interrupt program		25 programs		
Comment input function (* Note 5)		not available	available	not available
Sampling trace function (* Note 6)		not available	available	available
Clock/calendar function		year, month, day, hour, minute, second and day of week		
Link functions		PC link, computer link, data transfer, remote programming and MODEM capability		
Self-diagnostic function		watching dog timer, memory malfunction detection, I/O malfunction detection, backup battery malfunction detection, program syntax check, etc.		
Other functions		program edition during RUN **(* Note 7)**, forced ON/OFF, interrupt input, test run, constant scan and machine language program option		
Memory backup time (lithium battery storage time)		AFP3210C−F : min. 17,000 hours (typical value : approx. 34,000 hours) AFP3211C−F, AFP3220C−F : min. 10,000 hours (typical value : approx. 22,000 hours)		

☞ next page

☞ Notes

- **(*1): The capacity will differ depending on the system register settings.**
- **(*2): Can also be used as an internal relay.**
- **(*3): Hold or non–hold type can be set.**
- **(*4): Can also be used as a data register.**
- **(*5): Max. 2,730 points. Up to 12 characters per 1 comment.**
- **(*6): Can perform sampling up to a maximum of 1,000 samples (4,000 words) for data of 16 contacts and 3 words.**
- **(*7): During the ladder symbol input of NPST–GR, program edits during RUN cannot be performed.**

Appendix B

Table of System Registers

B.1 System Registers

System registers are used to set values (parameters) which determine operation ranges and functions used. Set values based on the use and specifications of your program. There is no need to set system registers for functions which will not be used.

Types of system register

- **Allocation of user memory (System registers 0 and 1)**
  These registers set the size of the program area and file register area, allowing the user memory area to be configured for the environment used. The size of the memory area will vary depending on the CPU type.
- **Allocation of timers and counters (System register 5)**
  The number of timers and counters is set by specifying the starting counter number.
- **Hold/non-hold type settings (System registers 6 to 18)**
  When these registers are set to “hold type”, the values in the relays and data memory will be retained even if the system is switched to PROG. mode or the power is turned OFF. If set to “non-hold type”, the values will be cleared to “0”.
- **Operation mode settings for errors (System registers 4 and 20 to 28)**
  Set the operation mode effective when errors such as duplicated use of output and operation error occur.
- **Timers settings (System registers 29 to 34)**
  Set time-out error detection time and the constant scan time.
- **MEWNET-F (remote I/O) operation settings (System registers 35 and 36)**
  These registers are used to select whether or not to wait for a slave station connection when the remote I/O is started, and the remote I/O update timing.
- **MEWNET−P/−W PC link settings (System registers 40 to 45, 46 and 50 to 55)**
  These settings are for using link relays and link registers for MEWNET−P/−W PC link communication.
  Note that the initial setting is “no PC link communication”.
- **MEWNET−H PC link settings (System register 49)**
  Set the processing capacity per scan for the PC link communication of the MEWNET−H link system.
- **Communication port settings (System registers 410 to 418)**
  Set these registers when the tool port or COM (RS232C) port is to be used for communication. The registers can only be set using NPST-GR.

Checking and changing system register settings

If you are going to use a value which is already set (the value which appears when read), there is no need to write it again.

Using NPST-GR software

Procedure:

1. **Set the mode selector of the FP3/FP10SH CPU to PROG.**
2. **Select the “SYSTEM REGISTER” in “PLC CONFIGURATION” option from the NPST menu.**
3. **Select the function to be set in the the “SYSTEM REGISTER” in “PLC CONFIGURATION” screen. The value set in the selected system register will appear.**
4. **To change a set value, write the new value as indicated in the system register table.**
5. **After setting, press <F1> key and type <Y> key to save the revised settings to the FP3/FP10SH CPU.**

Using FP programmer II Ver.2

Procedure:

1. **Set the mode selector of the FP3/FP10SH CPU to PROG.**
2. **Press the keys on the FP programmer II Ver.2, as shown below.**

   ACLR (–) OP 5 0 ENT

3. **Specify the register number (e.g. No.26) for the parameter to be set and read the parameter.**
   The value set in the selected register (e.g. No.26) will be displayed.

   2 6 READ B

4. **To change the set value, press the <CLR (clear)> key and write the new value as indicated in the system register table using decimal (K) or hexdecimal (H) constant.**

☞ **Note**

Be aware that the FP programmer II Ver.2 cannot make settings at the FP10SH system register.

Precautions for system register setting

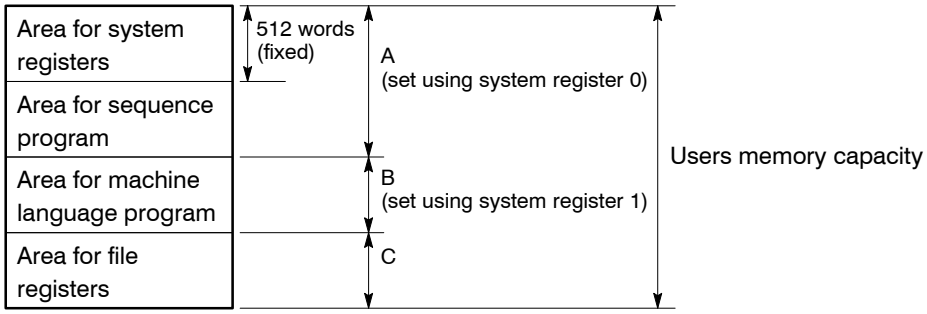
Sytem register settings are effective from the time they are set.
However, modem connection settings become effective when the power is turned OFF and ON.

When the initialized operation is performed, all set system register values will be initialized.

B.2 Content of System Register Settings

Allocation of user memory (system registers 0 and 1)

The configuration of user memory of FP3 CPU is as follows:



Be sure to set the A and B (system registers 0 and 1) as even numbers.

The area remaining in A after 512 words are subtracted is the sequence program area that can actually be used.

The file register area C is the area that remains after A and B have been subtracted from the user memory capacity.

☞ **Note**

You cannot change the program capacity for FP10SH with the system register settings.

FP3 (10 K)

Users memory capacity : 10 K words
Setting range of A : 2 K to 10 K words (default value: 8 K)
Setting range of B : 0 to 8 K words (default value: 0)

Allocate so that A + B ≦ 10.

Allocation example: The values of C when B = 0.

A	Area for sequence program (1024 × A–512)	Area for file registers (C)
2	1,535 steps	8,189 words
4	3,583 steps	6,141 words
6	5,631 steps	4,093 words
8	**7,679 steps**	**2,045 words**
10	9,727 steps	0 words

Setting example for each area

- **When not using the machine language program area**
  Refer to the tables on the previous page.
- **When using the machine language program area**

B	Area for machine language program
2	2,048 words
4	4,096 words
6	6,144 words
8	7,679 words
10	10,240 words
12	12,288 words

B	Area for machine language program
14	14,336 words
16	16,384 words
18	18,432 words
20	20,480 words
22	22,528 words

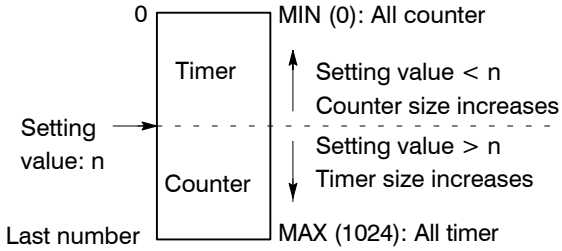
For example, for the FP3 (16K steps type), when the area for the sequence program (A) is set to 10K words, the area for the machine language program (B) can be set up to 6K words.

In this situation, the file register can be used up to 8,189 words.

Setting the number of timers and counters (system register 5)

Timers and counters share the same area. If the method of dividing the area is changed, the number of timers and counters will also change.

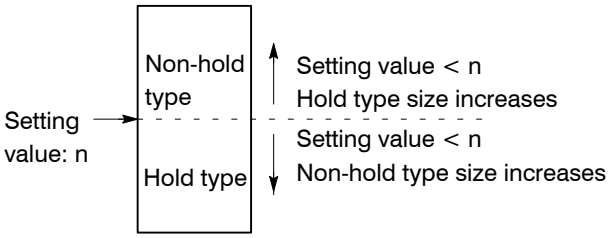
Type	Total point numbers	Default value of system register 5	Timer	Counter
FP3	256 points	200	200 points (No. 0 to 199)	56 points (No. 200 to 255)
FP10SH	3,072 points	3000	3000 points (No. 0 to 2999)	72 points (No. 3000 to 3071)



For normal situations, set the system registers 5 and 6 to the same value. This sets the timer to a non-hold type and counter to a hold type.

By setting system register 5 to “0,” the whole area becomes the counter. Also, by setting it to the value 1 higher than the last number (i.e. 256 for the FP3), the whole area becomes the timer.

Hold type area starting address (system registers 6 to 13)
Set each relay and register to a hold type or non-hold type.



For normal situations, set the system registers 5 and 6 to the same value. This sets the timer to a non-hold type and counter to a hold type.

By setting this value to the first number, the whole area becomes hold type. Also, by setting it to the value 1 higher than the last number (i.e. 2048 for the FP3 data register), the whole area becomes non-hold type.

The relays and registers for links not specified in the send area of system registers 40 to 55 are non-hold type regardless of what is set here.

For the FP10SH, the index registers can be set to hold type or non–hold type.
The register numbers and settings are related as shown below.

Bank number	Setting for I0 to ID	Bank number	Setting for I0 to ID
Bank 0	0 to 13	**Bank 8**	112 to 125
Bank 1	14 to 27	**Bank 9**	126 to 139
Bank 2	28 to 41	**Bank A**	140 to 153
Bank 3	42 to 45	**Bank B**	154 to 167
Bank 4	56 to 69	**Bank C**	168 to 181
Bank 5	70 to 83	**Bank D**	182 to 195
Bank 6	84 to 97	**Bank E**	196 to 209
Bank 7	98 to 111	**Bank F**	210 to 223

Default value of hold type area setting

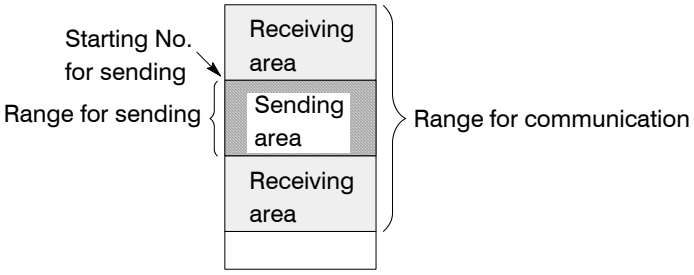
Area \ Type	FP3	FP10SH
Timer	All non–hold type	
Counter	All hold type	
Internal relay	Non–hold type: 60 words (WR0 to WR59)	Non–hold type: 500 words (WR0 to WR499)
	Hold type: 38 words (WR60 to WR97)	Hold type: 387 words (WR500 to WR886)
Data register	All hold type	
File register	All hold type	
Link relay for MEWNET–W/P	All hold type	
Link register for MEWNET–W/P	All hold type	
Link relay for MEWNET–H	All hold type	
Link register for MEWNET–H	All hold type	
Index register for FP10SH	All hold type	

MEWNET–W/–P PC link setting

For PC link (W/P) 0: System register 40 to 45

For PC link (W/P) 1: System register 50 to 55

Regarding the link relays and link data registers, specify the range for communication and divide it up for sending and receiving.



The default settings have the range for communication (system register 40, 41, 50, and 51) set to 0 so that PC link communication is not possible.

If the range for sending (system register 43, 45, 53, and 55) is set to 0, the range for communication will all be for receiving.

The link relay and link data register ranges not used for communication, can each be used as internal relays and data registers.

B.3 Table of System Registers (for FP3)

Item	Address	Name of system register	Default value	Description		
Allocation of user memory	**0**	**Sequence program area capacity setting**	8 K words (K8)	FP3 (10 K): 2 to 10 K words (K2 to K10) FP3 (16 K): 2 to 16 K words (K2 to K16)		* See page B – 6
	1	**Machine language program area capacity setting**	0 word (K0)	FP3 (10 K): 0 to 8 K words (K0 to K8) FP3 (16 K): 0 to 14 K words (K0 to K14)		
	2	**Comment capacity setting**	3 (K3)	Use default value 3 (K3)		
Action on error	**4**	**Battery error alarm (* Note)**	Enabled (K0)	Enabled: (K0) When a battery problem occurs, a self-diagnostic error is issued and the ERROR LED lights. (BATT. LED lights.) Disabled: (K1) When a battery problem occurs, a self-diagnostic error is not issued and the ERROR LED does not light. (BATT. LED lights.)		
Hold/ Non-hold	**5**	**Counter starting address (setting the number of timers and counters)**	200 (K200)	0 to 256 (K0 to K256)	Set the system registers 5 and 6 to the same value.	* See page B – 7 and B – 8
	6	**Hold area starting address setting for timer/counter**	200 (K200)	0 to 256 (K0 to K256)		
	7	**Hold area starting address setting for internal relays (in word units)**	60 (K60)	0 to 98 (K0 to K98)		
	8	**Hold area starting address setting for data registers**	0 (K0)	0 to 2048 (K0 to K2048)		
	9	**Hold area starting address setting for file registers**	0 (K0)	FP3 (10 K): 0 to 8189 (K0 to K8189) FP3 (16 K): 0 to 22525 (K0 to K22525)		
	10	**Hold area starting address setting for MEWNET–W/–P link relays (for PC link 0)**	0 (K0)	0 to 64 (K0 to K64)		

☞ **Notes**

- **The number in the parentheses of default value and description columns shows the setting value when the FP programmer II Ver.2 is operated.**
- **The system register 4 is available for FP3 with CPU version 4.4 or later.**

☞ next page

Item	Address	Name of system register	Default value	Description	
Hold/ Non-hold	**11**	**Hold area starting address setting for MEWNET–W/–P link relays (for PC link 1)**	64 (K64)	64 to 128 (K64 to K128)	* See page B – 8
	12	**Hold area starting address setting for MEWNET–W/–P link data registers (for PC link 0)**	0 (K0)	0 to 128 (K0 to K128)	
	13	**Hold area starting address setting for MEWNET–W/–P link data registers (for PC link 1)**	128 (K128)	128 to 256 (K128 to K256)	
	14	**Hold or non-hold setting for step ladder process**	Non-hold (K1)	Hold (K0)/non-hold (K1)	
Action on error	**20**	**Disable or enable setting for duplicated output**	Disable (K0)	Disable (K0)/enable (K1)	
	21	**Operation setting when I/O error occurs**	Stop (K0)	Stop (K0)/continuation (K1)	
	22	**Operation settings when an intelligent unit error is occurs**	Stop (K0)	Stop (K0)/continuation (K1)	
	23	**Operation settings when an I/O verification error is occurs**	Stop (K0)	Stop (K0)/continuation (K1)	
	26	**Operation settings when an operation error occurs**	Stop (K0)	Stop (K0)/continuation (K1)	
	27	**Operation settings when communication error occurs in the MEWNET-F (remote I/O) system**	Stop (K0)	Stop (K0)/continuation (K1)	
	28	**Operation settings when error occurs in the slave station of the MEWNET-F system**	Stop (K0)	Stop (K0)/continuation (K1)	

☞ **Note**

The number in the parentheses of default value and description columns shows the setting value when the FP programmer II Ver.2 is operated.

B.3 Table of System Registers (for FP3)

Item	Address	Name of system register	Default value	Description
Time setting	**31**	**Multi-frame communication time settings in the computer link function**	6500 ms (K2600)	10.0 ms to 81900.0 ms (K4 to K32760) Use of default setting (6500 ms) is recommended. In the FP programmer II Ver.2, setting time can be obtained using the formula “Set time” = “Set value” (K4 to K32760) × 2.5 (ms)
	32	**Communication time setting for the F145 (SEND)/P145 (PSEND), F146 (RECV)/P146 (PRECV), F152 (RMRD)/P152 (PRMRD) and F153 (RMWT)/ P153 (PRMWT) instructions**	2000 ms (K800)	10.0 ms to 81900.0 ms (K4 to K32760) Use of default setting (2000 ms) is recommended. In the FP programmer II Ver.2, setting time can be obtained using the formula “Set time” = “Set value” (K4 to K32760) × 2.5 (ms)
	33	**Program block-editing time in the RUN mode (FP3 CPU Ver.3.0 or later)**	10000 μs (K5000)	800.0 ms to 52428.0 ms Use of default setting (10000 μs) is recommended. In the NPST–GR, setting range: 2000 to 131070 μs In the FP programmer II Ver.2, – setting range:2000 to 65534 μs (K1000 to K32767) – setting range:65536 to 131070 μs (H8000 to HFFFF) Set this system register using an even number. In the FP programmer II Ver.2, enter the set value (equal to the value divided by 2).
	34	**Constant scan time setting (FP3 CPU Ver.4.4 or later)**	0: Normal scan (K0)	2.5 ms to 637.5 ms (K1 to K255): Scans once each specified time interval. 0 (K0): Normal scan In the FP programmer II Ver.2, setting time can be obtained using the formula “Set time” = “Set value” (K1 to K255) × 2.5 (ms)

☞ **Note**

The number in the parentheses of default value and description columns shows the setting value when the FP programmer II Ver.2 is operated.

Item	Address	Name of system register		Default value	Description	
Remote I/O control	**35**	**Operation mode setting when the MEWNET-F system is used**		Enabled (wait for connec-tion) (K1)	Enabled: (K1) CPU starts operation after all the slave stations are recognized. Disabled: (K0) CPU starts operation without waiting for slave station connections Only effective when registering remote I/O allocation.	
	36	**Data updating mode settings for MEWNET-F system**		Scan synchro-nous (K0)	Scan asynchronous mode (K1)/ Scan synchronous mode (K0)	
PC link 0 setting	**40**	**PC link 0 settings for MEWNET−W/ MEWNET−P link system**	**Size of link relays used for PC link**	0 (K0)	0 to 64 words (K0 to K64)	* See page B − 9
	41		**Size of link data registers used for PC link**	0 (K0)	0 to 128 words (K0 to K128)	
	42		**Send area starting address of link relay**	0 (K0)	0 to 63 (K0 to K63)	
	43		**Size of link relays used for send area**	0 (K0)	0 to 64 words (K0 to K64)	
	44		**Send area starting address of link data register**	0 (K0)	0 to 127 (K0 to K127)	
	45		**Size of link data registers used for send area**	0 (K0)	0 to 127 words (K0 to K127)	

☞ **Note**

The number in the parentheses of default value and description columns shows the setting value when the FP programmer II Ver.2 is operated.

B.3 Table of System Registers (for FP3)

Item	Address	Name of system register		Default value	Description	
PC link 0 setting	**46**	**PC link 0 and 1 allocation setting for MEWNET–W/ MEWNET–P link system (FP3 CPU Ver.4.4 or later)**		Normal allocation (K0)	Normal allocation (K0): (PC link 0 for the link unit with a smaller slot number and PC link 1 for one with a larger slot number) Reverse allocation (K1): (PC link 1 for the link unit with a smaller slot number and PC link 0 for one with a larger slot number)	
MEW-NET–H setting	**49**	**Processing capacity setting for PC link of MEWNET–H link system**		0 (K0)	0 (K0): All data in a scan 1 to 65535 (K1 to K65535): Setting processing capacity per scan can be obtained using the formula “Capacity” = “Set value” × 256 bytes	
PC link 1 setting	**50**	**PC link 1 settings for MEWNET–W/ MEWNET–P link system**	**Size of link relays used for PC link**	0 (K0)	0 to 64 words (K0 to K64)	* See page B – 9
	51		**Size of link data registers used for PC link**	0 (K0)	0 to 128 words (K0 to K128)	
	52		**Send area starting address of link relay**	64 (K64)	64 to 127 (K64 to K127)	
	53		**Size of link relays used for send area**	0 (K0)	0 to 64 words (K0 to K64)	
	54		**Send area starting address of link data register**	128 (K128)	128 to 255 (K128 to K255)	
	55		**Size of link data registers used for send area**	0 (K0)	0 to 127 words (K0 to K127)	

☞ **Note**

The number in the parentheses of default value and description columns shows the setting value when the FP programmer II Ver.2 is operated.

Item	Address	Name of system register	Default value	Description
Tool port setting	**410**	**Unit number setting for tool port (when connecting C-NET) (FP3 CPU Ver.4.4 or later)**	1 (K1)	1 to 32 (unit no. 1 to 32)
	411	**Communication format setting for tool port (FP3 CPU Ver.4.4 or later)**	Communication format (character bit): 8 bits MODEM communication: Disabled	Character bits: 7 bits/8 bits MODEM communication: Enabled/ Disabled When connecting a MODEM, set the unit number to 1 with system register 410.

☞ **Notes**

- **The number in the parentheses of default value and description columns shows the setting value when the FP programmer II Ver.2 is operated.**
- **System registers 410 and 411 should be set using NPST–GR Ver.3 or later. They cannnot be changed using FP programmer II Ver.2.**

B.4 Table of System Registers (for FP10SH)

Item	Address	Name of system register		Default value	Description
Action on error	**4**	**Battery error alarm**		Enabled	Enabled: When a battery problem occurs, a self-diagnostic error is issued and the ERROR LED lights. Disabled: When a battery problem occurs, a self-diagnostic error is not issued and the ERROR LED does not light. (BATT. LED lights.)
		Memory area contents setting at INITIALIZE position	**Internal relay (R)**	Cleared	Cleared: When the initialize/test switch is set to INITIALIZE position while in the PROG. mode, you can specify the type of memory to be cleared. Not cleared: When the initialize/test switch is set to INITIALIZE position while in the PROG. mode, you can specify the type of memory to be not cleared.
			Link relay (L)	Cleared	
			Timers/ Counters (T, C, SV, EV)	Cleared	
			Data register (DT)	Cleared	
			Link data register (LD)	Cleared	
			File register (FL)	Cleared	
			Index register (I)	Cleared	
			Error alarm relay (E)	Cleared	
		Differential type instructions setting between MC and MCE instructions		0 (conventional)	0 (conventional): Holds preceded result in the MC and MCE instruction set 1 (new): Disregards preceded result in the MC and MCE instruction set (See section B.4.1)
		TM instruction operation setting		0 (conventional)	0 (conventional): Scan synchronous 1 (new): Scan asynchronous
		Index modifier check setting		Enabled	Enabled: Checks for overflow of the index modifier area, and performs normal processing. Disabled: Performs processing without checking for overflow of the index modifier area.

Item	Address	Name of system register	Default value	Description		
Hold/ Non-hold	**5**	**Counter starting address (setting the number of timers and counters)**	3000	0 to 3072	Set the system registers 5 and 6 to the same value.	* See page B – 7 to B – 9
	6	**Hold area starting address setting for timer/counter**	3000	0 to 3072		
	7	**Hold area starting address setting for internal relays (in word units)**	500	0 to 876		
	8	**Hold area starting address setting for data registers**	0	0 to 10240		
	9	**Hold area starting address setting for file registers**	0	0 to 32765		
	10	**Hold area starting address setting for MEWNET–W/–P link relays (for PC link 0)**	0	0 to 64		
	11	**Hold area starting address setting for MEWNET–W/–P link relays (for PC link 1)**	64	64 to 128		
	12	**Hold area starting address setting for MEWNET–W/–P link data registers (for PC link 0)**	0	0 to 128		
	13	**Hold area starting address setting for MEWNET–W/–P link data registers (for PC link 1)**	128	128 to 256		
	14	**Hold or non-hold setting for step ladder process**	Non-hold	Hold/non-hold		
	16	**Hold area starting address setting for MEWNET–H link relays**	128	128 to 640		
	17	**Hold area starting address setting for MEWNET–H link data registers**	256	256 to 8448		
	18	**Hold area starting address setting for index register**	0	0 to 224		
Action on error	**20**	**Disable or enable setting for duplicated output**	Disable	Disable/enable		
	21	**Operation settings when MEWNET–TR master unit error occurs**	Stop	Stop/continuation		
	22	**Operation settings when an intelligent unit error occurs**	Stop	Stop/continuation		
	23	**Operation settings when an I/O verification error occurs**	Stop	Stop/continuation		
	24	**Operation settings when a system watching dog timer error occurs**	Stop	Stop/continuation Set the time–out time for watching dog timer with system register 30.		

B.4 Table of System Registers (for FP10SH)

Item	Address	Name of system register	Default value	Description
Action on error	**26**	**Operation settings when an operation error occurs**	Stop	Stop/continuation
	27	**Operation settings when communication error occurs in the MEWNET-F (remote I/O) system**	Stop	Stop/continuation
	28	**Operation settings when error occurs in the slave station of the MEWNET-F system**	Stop	Stop/continuation
Time setting	**29**	**Operation time setting for peripheral tasks**	300 (240 μs)	0 to 65535 (0 to 52428 μs) The setting for this system register is effective in the RUN mode only. In the PROG. mode and “0” setting, the allowable duration of time used for peripheral tasks is set at 52428 μs. Setting time can be obtained using the formula “Set time” = “Set value” × 0.8 (μs)
	30	**Time–out time setting of system watching dog timer**	1000 (100 ms)	4 to 6400 (0.4 to 640 ms) Setting time can be obtained using the formula “Set time” =“Set value” × 0.1 (ms)
	31	**Multi-frame communication time settings in the computer link function and communication time setting for data sending buffer**	2600 (6.5 s)	4 to 32767 (0.01 to 81.9175 s) Use of default setting (6.5 s) is recommended. Setting time can be obtained using the formula “Set time” =“Set value” × 2.5 (ms)
	32	**Communication time setting for the F145 (SEND)/P145 (PSEND), F146 (RECV)/P146 (PRECV), F152 (RMRD)/P152 (PRMRD) and F153 (RMWT)/ P153 (PRMWT) instructions**	4000 (10 s)	4 to 32767 (0.01 to 81.9175 s) Use of default setting (10 s) is recommended. Setting time can be obtained using the formula “Set time” =“Set value” × 2.5 (ms)
	33	**Effective time setting for monitoring**	65535 (163.8375 s)	1000 to 65535 (2.5 to 163.8375 s) Use of default setting (163.8375 s) is recommended. Setting time can be obtained using the formula “Set time” =“Set value” × 2.5 (ms)
	34	**Constant scan time setting**	0: Normal scan	1 to 64000 (0.1 to 6400 ms): Scans once each specified time interval. 0: Normal scan Setting time can be obtained using the formula “Set time” =“Set value” × 0.1 (ms)

Item	Address	Name of system register		Default value	Description	
Remote I/O control	**35**	**Operation mode setting when the MEWNET-F system is used**		Enabled (wait for connec-tion)	Enabled: CPU starts operation after all the slave stations are recognized. Disabled: CPU starts operation without waiting for slave station connections Only effective when registering remote I/O allocation.	
	36	**Data updating mode settings for MEWNET-F system**		Scan synchro-nous	Scan synchronous mode/ Scan asynchronous mode	
PC link 0 setting	**40**	**PC link 0 settings for MEWNET−W/−P link system**	**Size of link relays used for PC link**	0	0 to 64 words	* See page B − 9
	41		**Size of link data registers used for PC link**	0	0 to 128 words	
	42		**Send area starting address of link relay**	0	0 to 63	
	43		**Size of link relays used for send area**	0	0 to 64 words	
	44		**Send area starting address of link data register**	0	0 to 127	
	45		**Size of link data registers used for send area**	0	0 to 127 words	
	46	**PC link 0 and 1 allocation setting for MEWNET−W/−P link system**		Normal alloca-tion	Normal allocation: (PC link 0 for the link unit with a smaller slot number and PC link 1 for one with a larger slot number) Reverse allocation: (PC link 1 for the link unit with a smaller slot number and PC link 0 for one with a larger slot number)	

☞ **Note**

System register 46 should be set using NPST−GR Ver.4 or later.

B.4 Table of System Registers (for FP10SH)

Item	Address	Name of system register		Default value	Description	
MEWNET –H setting	**49**	**Processing capacity setting for PC link of MEWNET–H link system**		4 (1024 bytes per scan)	0: All data in a scan 1 to 65535: Setting processing capacity per scan can be obtained using the formula “Capacity” = “Set value” × 256 bytes	
PC link 1 setting	**50**	**PC link 1 settings for MEWNET–W/ –P link system**	**Size of link relays used for PC link**	0	0 to 64 words	* See page B – 9
	51		**Size of link data registers used for PC link**	0	0 to 128 words	
	52		**Send area starting address of link relay**	64	64 to 127	
	53		**Size of link relays used for send area**	0	0 to 64 words	
	54		**Send area starting address of link data register**	128	128 to 255	
	55		**Size of link data registers used for send area**	0	0 to 127 words	
General (COM) port setting	**412**	**Communication method setting for COM (RS232C) port**		Comput-er link	COMPUTER LNK: computer link mode (when connecting C-NET) GENERAL: serial data communication mode (general port)	

☞ **Note**

System register 412 should be set using NPST–GR Ver.4.0 or later.

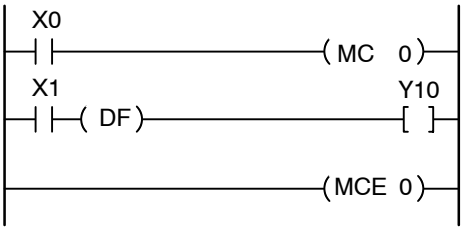
Item	Address	Name of system register	Default value	Description	
General (COM) port setting	**414**	**Baud rate setting for the tool port**	0 (19200 bps)	When the operation condition switches (DIP switch) SW1 on the rear of the CPU is OFF, the baud rate setting is effective. 0: 19200 bps 5: 19200 bps 1: 1200 bps 6: 38400 bps 2: 2400 bps 7: 57600 bps 3: 4800 bps 8: 115200 bps 4: 9600 bps	
General commu-nication setting	**417**	**Starting address setting for data received of serial data communication mode**	0	0 to 10240	For details about its usage, refer to the **F144 (TRNS)/P144 (PTRNS)** instructions on programming manual.
	418	**Buffer capacity setting for data received of serial data communication mode**	1024	0 to 1024 words	

☞ **Note**

System registers 414, 417 and 418 should be set using NPST–GR Ver.4.0 or later.

B.4.1 Operation of DF Instruction Between MC and MCE Instructions

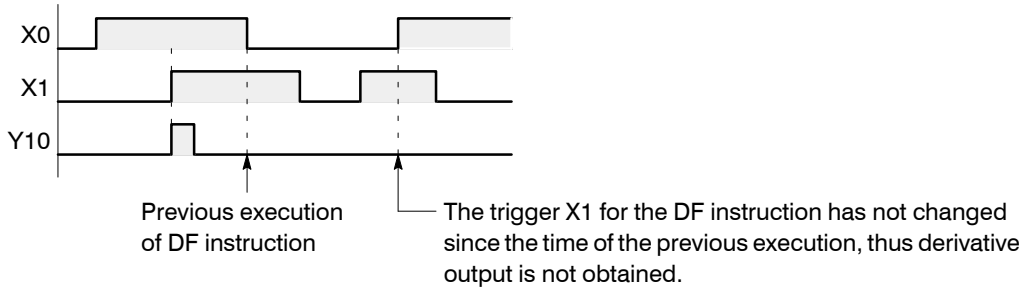
When a leading edge detection instruction (**DF** instruction) is used with the **MC** and **MCE** instructions, the derivative output may change as follows depending on the trigger of **MC** instruction and input timing of **DF** instruction. Take care regarding this point.



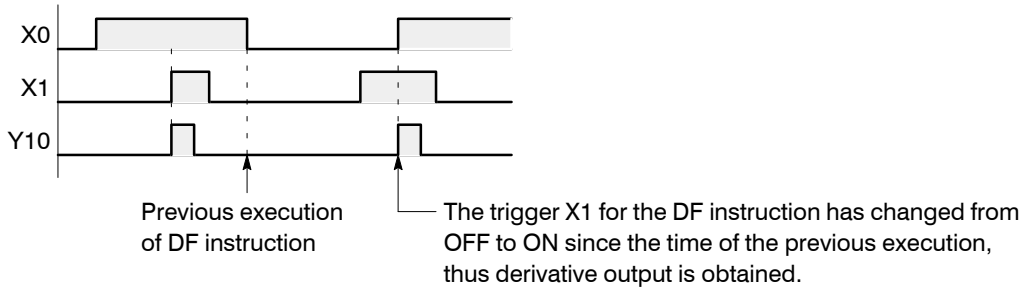
Example 1

When system register 4 sets 0 (conventional)

Time chart 1



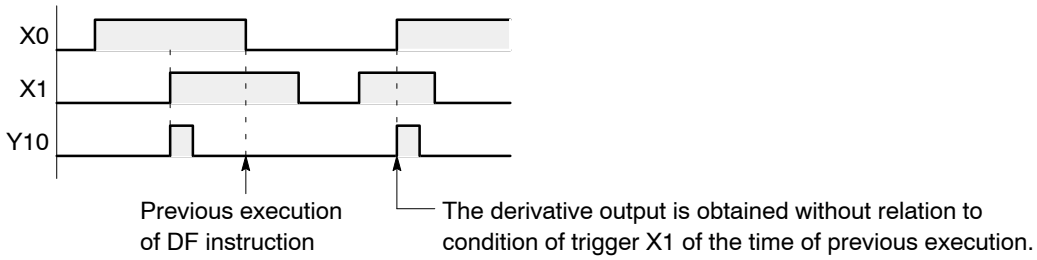
Time chart 2



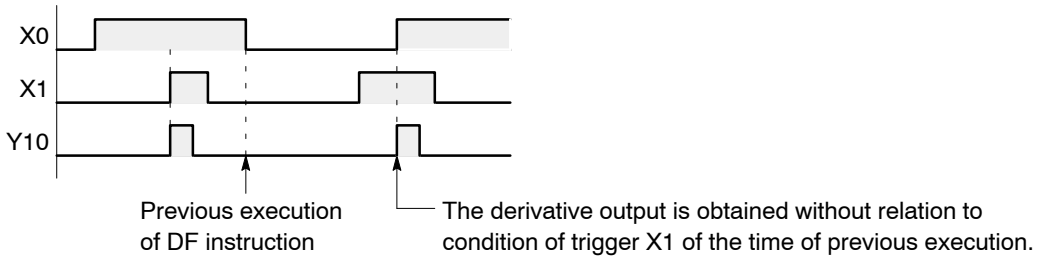
Example 2

When system register 4 sets 1 (new)

Time chart 1



Time chart 2



B.4 Table of System Registers (for FP10SH)

Appendix C

Table of Relays, Memory Areas and Constants

C.1 Relays, Memory Areas and Constants for FP3

Item			Numbering	Function
Relays	**External input relay**	**X**	2,048 points (X0 to X127F)	Turn ON/OFF based on external input.
	External output relay	**Y**	2,048 points (Y0 to Y127F)	Externally outputs ON/OFF state.
	Internal relay (* Note 1)	**R**	1,568 points (R0 to R97F)	Relay which turns ON/OFF only within program.
	Link relay (* Note 1)	**L**	2,048 points (L0 to L127F)	This relay is a shared relay used for MEWNET link system.
	Timer (* Notes 1 and 2)	**T**	256 points (T0 to T199/ C200 to C255)	If a **TM** instruction has timed out, the contact with the same number turns ON.
	Counter (* Notes 1 and 2)	**C**		If a **CT** instruction has counted up, the contact with the same number turns ON.
	Special internal relay	**R**	176 points (R9000 to R910F)	Relay which turns ON/OFF based on specific conditions and is used as a flag **(* Appendix D)**.
Memory areas	**External input relay**	**WX**	128 words (WX0 to WX127)	Code for specifying 16 external input points as one word (16 bits) of data.
	External output relay	**WY**	128 words (WY0 to WY127)	Code for specifying 16 external output points as one word (16 bits) of data.
	Internal relay	**WR**	98 words (WR0 to WR97)	Code for specifying 16 internal relay points as one word (16 bits) of data.
	Link relay	**WL**	128 words (WL0 to WL127)	Code for specifying 16 link relay points as one word (16 bits) of data.
	Data register (* Note 1)	**DT**	2,048 words (DT0 to DT2047)	Data memory used in program. Data is handled in 16-bit units (one word).
	Link data register (* Note 1)	**LD**	256 words (LD0 to LD255)	This is a shared data memory which is used within the MEWNET link system. Data is handled in 16-bit units (one word).
	Timer/Counter set value area (* Note 1)	**SV**	256 words (SV0 to SV255)	Data memory for storing a target value of a timer and an initial value of a counter. Stores by timer/counter number.

☞ next page

Item		Numbering	Function
Control instruction point	**Master control relay points (MCR)**	64 points	
	Number of labels (JP and LOOP)	256 points	
	Number of step ladder (* Note 4)	1,000 stages	
	Number of subroutine	100 subroutines	
	Number of interrupt program	25 programs	
Memory areas	**Timer/Counter elapsed value area (* Note 1)** EV	256 words (EV0 to EV255)	Data memory for storing the elapsed value during operation of a timer/counter. Stores by timer/ counter number.
	File register (* Notes 1 and 3) FL	FP3 (16 K): 8,189 to 2,2525 words (FL0 to FL22524) FP3 (10 K): 0 to 8,189 words (FL0 to FL8188)	Data memory used in program. Data is handled in 16-bit units (one word).
	Special data register DT	256 words (DT9000 to DT9255)	Data memory for storing specific data. Various settings and error codes are stored **(* Appendix E)**.
	Index register IX IY	2 words (IX, IY)	Register can be used as an address of memory area and constants modifier.
Constant	**Decimal constants** K	K–32768 to K32767 (for 16-bit operation)	
		K–2147483648 to K2147483647 (for 32-bit operation)	
	Hexadecimal constants H	H0 to HFFFF (for 16-bit operation)	
		H0 to HFFFFFFFF (for 32-bit operation)	

☞ **Notes**

- **(*1): There are two unit types, the hold type that saves the conditions that exist just before turning the power OFF or changing form the RUN mode to PROG. mode, and the non-hold type that resets them. The selection of hold type and non-hold type can be change by the setting of system register (* section B.1).**
- **(*2): The points for the timer and counter can be changed by the setting of system register 5. The numbers given in the table are numbers when system register 5 is at its default setting. For more details, refer to page B – 7.**

- **(*3): The size of the file register varies depending on the settings of system registers 0 and 1. For details, refer to page B – 6.**
- **(*4): Hold or non-hold type can be set.**

C.2 Relays, Memory Areas and Constants for FP10SH

Item			Numbering	Function
Relays	**External input relay**	**X**	8,192 points (X0 to X511F)	Turn ON/OFF based on external input.
	External output relay	**Y**	8,192 points (Y0 to Y511F)	Externally outputs ON/OFF state.
	Internal relay (* Note 1)	**R**	14,192 points (R0 to R886F)	Relay which turns ON/OFF only within program.
	Link relay (* Note 1)	**L**	10,240 points (L0 to L639F)	This relay is a shared relay used for MEWNET link system.
	Timer (* Notes 1 and 2)	**T**	3,072 points (T0 to T2999/ C3000 to C3071)	If a **TM** instruction has timed out, the contact with the same number turns ON.
	Counter (* Notes 1 and 2)	**C**		If a **CT** instruction has counted up, the contact with the same number turns ON.
	Pulse relay	**P**	2,048 points (P0 to P127F)	This relay is used to turn ON only for one scan duration programmed with the **OT**" and **OT**# instructions.
	Error alarm relay	**E**	2,048 points (E0 to E2047)	This relay is used to store occurrence of abnormalities. Its history is recorded in exclusive buffer (special data registers starting from DT90400). Program this relay so that it is turned ON at the time of abnormality.
	Special internal relay	**R**	176 points (R9000 to R910F)	Relay which turns ON/OFF based on specific conditions and is used as a flag **(* Appendix D)**.
Memory areas	**External input relay**	**WX**	512 words (WX0 to WX511)	Code for specifying 16 external input points as one word (16 bits) of data.
	External output relay	**WY**	512 words (WY0 to WY511)	Code for specifying 16 external output points as one word (16 bits) of data.
	Internal relay	**WR**	887 words (WR0 to WR886)	Code for specifying 16 internal relay points as one word (16 bits) of data.
	Link relay	**WL**	640 words (WL0 to WL639)	Code for specifying 16 link relay points as one word (16 bits) of data.
	Data register (* Note 1)	**DT**	10,240 words (DT0 to DT10239)	Data memory used in program. Data is handled in 16-bit units (one word).

☞ next page

Item		Numbering	Function
Memory areas	**Link data register (* Note 1)** LD	8,448 words (LD0 to LD8447)	This is a shared data memory which is used within the MEWNET link system. Data is handled in 16-bit units (one word).
	Timer/Counter set value area (* Note 1) SV	3,072 words (SV0 to SV3071)	Data memory for storing a target value of a timer and an initial value of a counter. Stores by timer/counter number.
	Timer/Counter elapsed value area (* Note 1) EV	3,072 words (EV0 to EV3071)	Data memory for storing the elapsed value during operation of a timer/counter. Stores by timer/ counter number.
	File register (* Note 1) FL	32,765 words (FL0 to FL32764)	Data memory used in program. Data is handled in 16-bit units (one word).
	Special data register DT	512 words (DT90000 to DT90511)	Data memory for storing specific data. Various settings and error codes are stored **(* Appendix E)**.
	Index register I	14 words ×16 banks (I0 to ID)	Register can be used as an address of memory area and constants modifier.
Control instruction point	**Master control relay points (MCR)**	256 points (when using the 90k step expansion memory, up to a total of 512 points can be used for the 1st and 2nd programs)	
	Number of labels (JP and LOOP)	256 points (when using the 90k step expansion memory, up to a total of 512 points can be used for the 1st and 2nd programs)	
	Number of step ladder (* Note 3)	1,000 steps (can only be used for the 1st program)	
	Number of subroutine	100 subroutines (can only be used for the 1st program)	
	Number of interrupt program	25 program (can only be used for the 1st program)	
Constant	**Decimal constants (integer type)** K	K–32768 to K32767 (for 16-bit operation)	
		K–2147483648 to K2147483647 (for 32-bit operation)	
	Hexadecimal constants H	H0 to HFFFF (for 16-bit operation)	
		H0 to HFFFFFFFF (for 32-bit operation)	
	Decimal constants (monorefined real number) f	f1.175494 × 10^{-38} to f3.402823 × 10^{38}	

☞ **Notes**

- **(*1): There are two unit types, the hold type that saves the conditions that exist just before turning the power OFF or changing form the RUN mode to PROG. mode, and the non-hold type that resets**

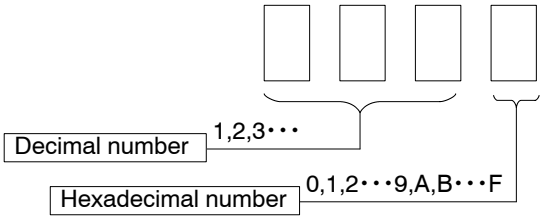
them. The selection of hold type and non-hold type can be change by the setting of system register (* section B.1).

- **(*2): The points for the timer and counter can be changed by the setting of system register 5. The numbers given in the table are numbers when system register 5 is at its default setting. For more details, refer to page B – 7.**
- **(*3): Hold or non-hold type can be set.**

C.3 Relay Numbers

External input relays (X), External output relays (Y), Internal relays (R), Link relays (L) and Pulse relays (P)

Since these relays are handled in units of 16 points, they are expressed as a combination of decimal and hexadecimal numbers as shown below.



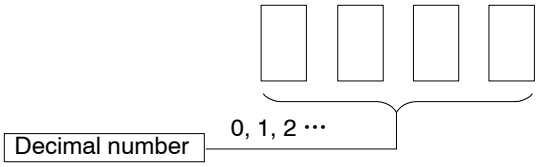
The maximum value that can be selected varies with each relay.

<Example> External input relay (X)

X0, X1 ..... XF
X10, X11 ..... X1F
X20, X21 ..... X2F
⁓ ⁓ ⁓
X1270, X1271 ..... X127F

Timers (T) and Counters (C)

The addresses for timer contacts (T) and counter contacts (C) are correspond to the **TM** (timer) and **CT** (counter) instruction numbers and expressed in decimals as shown below.



T0, T1 ..... T199
C200, C201 ..... C255

Counters and timers share the same area. The division of the area can be changed with system register 5. (The table and example are when settings are the default values.)

Error alarm relays (E)

The addresses for error alarm relays (E) are represented in only decimals.

E0, E1 ..... E2047

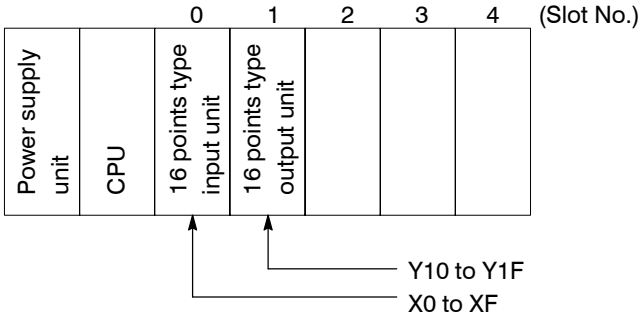
External input relay (X) and External output relay (Y)

Only relays with numbers actually allocated to input contacts can be used as external input relay (X).

Only relays with numbers actually allocated to output contacts can output as external output relay (Y). The external output relays (Y) which are not allocated can be used as internal relays.

Allocation of numbers is determined by the combination of input and output units used as shown in the example below.

<Example>



The 16 points external input relays X0 through XF are allotted for the 16-point type input unit for slot 0, and the 16 points external output relays Y10 through Y1F are allotted for the 16-point type output unit for slot 1.

The 16 points X10 through X1F cannot be used in this such combination.

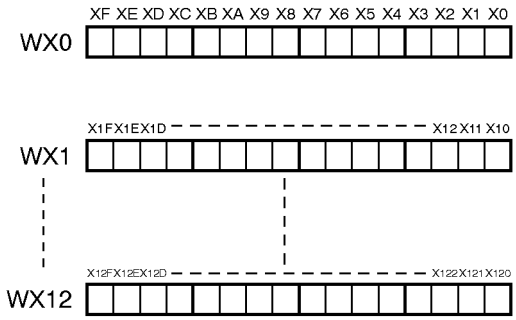
Combining input and output, 2,048 points can be used for the FP3 and 8,192 points for the FP10SH.

Relation of WX,WY, WR and WL to X, Y, R and L

WX, WY, WR, WL correspond respecitively to groups of 16 external input (X) points, 16 external output (Y) points, 16 internal relay (R) points and 16 link relay (L) points.

<Example> FP3 word external input relay (WX)

Each relay is composed of 16 external inputs (X) as shown below.



When the state of an external input (X) changes, the content of WX also changes.

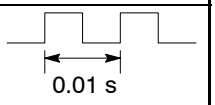
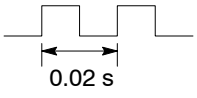
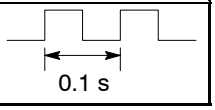
The error alarm relays (E) cannot be handled in units of words.

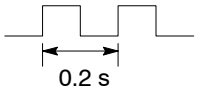
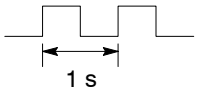
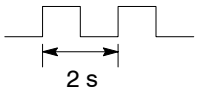
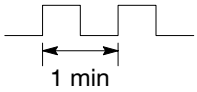
Appendix D

Table of Special Internal Relays

The special internal relays turn ON and OFF under special conditions. The ON and OFF states are not output externally. Writing is not possible with a programming tool or an instruction.

Address	Name	Description
R9000	**Self-diagnostic error flag**	Turns ON when a self-diagnostic error occurs. The self-diagnostic error code is stored in: – FP3: DT9000 – FP10SH: DT90000
R9001	————————	Not used
R9002	**MEWNET–TR master error flag**	Turns ON when a communication error occurs in the MEWNET–TR master unit. The slot, where the erroneous MEWNET–TR master unit is installed, can be checked using: – FP3: DT9002 and DT9003 – FP10SH: DT90002 and DT90003
R9003	**Intelligent unit error flag**	Turns ON when an error occurs in an intelligent unit. The slot number, where the erroneous intelligent unit is installed, can be checked using: – FP3: DT9006 and DT9007 – FP10SH: DT90006 and DT90007
R9004	**I/O verification error flag**	Turns ON when an I/O verification error occurs. The slot number of the I/O unit where the verification error was occurred is stored in: – FP3: DT9010 and DT9011 – FP10SH: DT90010 and DT90011
R9005	**Backup battery error flag (non-hold)**	Turns ON for an instant when a backup battery error occurs.
R9006	**Backup battery error flag (hold)**	Turns ON and keeps the ON state when a backup battery error occurs. To reset R9006, – turn the power to the FP3/FP10SH OFF and then turn it ON, – initialize the FP3/FP10SH, after removing the cause of error.
R9007	**Operation error flag (hold)**	Turns ON and keeps the ON state when an operation error occurs. The address where the error occurred is stored in: – FP3: DT9017 – FP10SH: DT90017 (indicates the first operation error which occurred).
R9008	**Operation error flag (non-hold)**	Turns ON for an instant when an operation error occurs. The address where the operation error occurred is stored in: – FP3: DT9018 – FP10SH: DT90018 The contents change each time a new error occurs.

Address	Name	Description
R9009	**Carry flag**	Turns ON for an instant, – when an overflow or underflow occurs. – when “1” is set by one of the shift instructions.
R900A	**> flag**	Turns ON for an instant when the compared results become larger in the comparison instructions **“F60 (CMP)/P60 (PCMP)**, **F61 (DCMP)/P61 (PDCMP)**, **F62 (WIN)/P62 (PWIN)** or **F63 (DWIN)/P63 (PDWIN).”**
R900B	**= flag**	Turns ON for an instant, – when the compared results are equal in the comparison instructions. – when the calculated results become 0 in the arithmetic instructions.
R900C	**< flag**	Turns ON for an instant when the compared results become smaller in the comparison instructions **“F60 (CMP)/ P60 (PCMP)**, **F61 (DCMP)/P61 (PDCMP)**, **F62 (WIN)/P62 (PWIN)** or **F63 (DWIN)/P63 (PDWIN).”**
R900D	**Auxiliary timer contact**	Turns ON when the set time elapses (set value reaches 0) in the timing operation of the **F137 (STMR)/F183 (DSTM)** auxiliary timer instruction. The R900D turns OFF when the trigger for auxiliary timer instruction turns OFF.
R900E	**Tool port error flag (Available PLC: FP10SH)**	Turns ON when communication error at tool port is occurred.
R900F	**Constant scan error flag**	Turns ON when scan time exceeds the time specified in system register 34 during constant scan execution.
R9010	**Always ON relay**	Always ON.
R9011	**Always OFF relay**	Always OFF.
R9012	**Scan pulse relay**	Turns ON and OFF alternately at each scan
R9013	**Initial ON pulse relay**	Turns ON only at the first scan in the operation. Turns OFF from the second scan and maintains the OFF state.
R9014	**Initial OFF pulse relay**	Turns OFF only at the first scan in the operation. Turns ON from the second scan and maintains the ON state.
R9015	**Step ladder initial ON pulse relay**	Turns ON for an instant only in the first scan of the process the moment the step ladder process is opened.
R9016	————	Not used
R9017	————	Not used
R9018	**0.01 s clock pulse relay**	Repeats ON/OFF operations in 0.01 s cycles. (ON : OFF = 0.005 s : 0.005 s) 
R9019	**0.02 s clock pulse relay**	Repeats ON/OFF operations in 0.02 s cycles. (ON : OFF = 0.01 s : 0.01 s) 
R901A	**0.1 s clock pulse relay**	Repeats ON/OFF operations in 0.1 s cycles. (ON : OFF = 0.05 s : 0.05 s) 

Address	Name	Description
R901B	**0.2 s clock pulse relay**	Repeats ON/OFF operations in 0.2 s cycles. (ON : OFF = 0.1 s : 0.1 s) 
R901C	**1 s clock pulse relay**	Repeats ON/OFF operations in 1 s cycles. (ON : OFF = 0.5 s : 0.5 s) 
R901D	**2 s clock pulse relay**	Repeats ON/OFF operations in 2 s cycles. (ON : OFF = 1 s : 1 s) 
R901E	**1 min clock pulse relay**	Repeats ON/OFF operations in 1 min cycles. (ON : OFF = 30 s : 30 s) 
R901F	————————	Not used
R9020	**RUN mode flag**	Turns OFF while the mode selector is set to PROG. mode. Turns ON while the mode selector is set to RUN.
R9021	**Test RUN mode flag**	Turns ON while the initialize/test switch of the CPU is set to TEST and mode selector is set to test RUN. Turns OFF during the normal RUN mode.
R9022	**Break flag**	Turns ON while the **BRK** instruction is executing or the step run is executing.
R9023	**Break enable flag**	Turns ON while the **BRK** instruction is enabled in the test RUN mode.
R9024	**Output update enable flag in the test RUN mode**	Turns ON while the output update is enabled in the test RUN mode.
R9025	**Single instruction flag**	Turns ON while the single instruction execution is selected in the test RUN mode.
R9026	**Message flag**	Turns ON while the **F149 (MSG)**/**P149 (PMSG)** instruction is executed.
R9027	**Remote mode flag**	Turns ON while the mode selector is set to REMOTE.
R9028	**Break clear flag**	Turns ON when the break operation is cleared.
R9029	**Forcing flag**	Turns ON during forced ON/OFF operation for I/O relay and timer/counter contacts.
R902A	**Interrupt flag**	Turns ON while the interrupt trigger is enabled by the **ICTL** instruction.
R902B	**Interrupt error flag**	Turns ON when an interrupt error occurs.
R902C	**Sampling point flag**	Turns OFF during instructed sampling. Turns ON while sampling is triggered by the periodical interrupt.
R902D	**Sampling trace end flag**	Turns ON when the sampling trace ends.
R902E	**Sampling trigger flag**	Turns ON when the trigger of the **F156 (STRG)**/**P156 (PSTGR)** instruction is turned ON.
R902F	**Sampling enable flag**	Turns ON when the starting point of sampling is specified.

Address	Name	Description
R9030	**F145 (SEND)/P145 (PSEND) and F146 (RECV)/P146 (PRECV) instruction executing flag**	Monitors if FP3/FP10SH is in the **F145 (SEND)/P145 (PSEND)** and **F146 (RECV)/P146 (PRECV)** instructions executable condition as follows: – OFF: None of the above mentioned instructions can be executed. (i.e., one of the above instructions is being executed.) – ON: One of the above mentioned instructions can be executed.
R9031	**F145 (SEND)/P145 (PSEND) and F146 (RECV)/P146 (PRECV) instruction end flag**	Monitors if an abnormality has been detected during the execution of the **F145 (SEND)/ P145 (PSEND)** and **F146 (RECV)/P146 (PRECV)** instructions as follows: – OFF: No abnormality detected. – ON: An abnormality detected. (communication error) The error code is stored in: – FP3: DT9039 – FP10SH: DT90039
R9032	**COM port mode flag (Available PLC: FP10SH)**	Monitors the mode of the COM port as: – ON: Serial data communication mode – OFF: Computer link mode
R9033	**F147 (PR) instruction flag**	Turns ON while a **F147 (PR)** instruction is executed.
R9034	**Editing in RUN mode flag**	Turns ON while editing a program in the RUN mode.
R9035	**F152 (RMRD)/P152 (PRMRD) and F153 (RMWT)/P153 (PRMWT) instruction execution flag**	Monitors if FP3/FP10SH is in the **F152 (RMRD)/P152 (PRMRD)** and **F153 (RMWT)/P153 (PRMWT)** instructions executable condition as follows: – OFF: None of the above mentioned instructions can be executed. (i.e., one of the above instructions is being executed.) – ON: One of the above mentioned instructions can be executed.
R9036	**F152 (RMRD)/P152 (PRMRD) and F153 (RMWT)/P153 (PRMWT) instruction end flag**	Monitors if an abnormality has been detected during the execution of the **F152 (RMRD)/P152 (PRMRD)** and **F153 (RMWT)/P153 (PRMWT)** instructions as follows: – OFF: No abnormality detected. – ON: An abnormality detected. (access error) The error code is stored in: – FP3: DT9036 – FP10SH: DT90036
R9037	**COM port communication error flag (Available PLC: FP10SH)**	Turns ON when the serial data communication error occurs using COM port. Turns OFF when data is being sent by the **F144 (TRNS)** instruction.

Address	Name	Description
R9038	**COM port receive flag (Available PLC: FP10SH)**	Turns ON when a terminator is received during the serial data communicating. (by the **F144 (TRNS)** instruction)
R9039	**COM port send flag (Available PLC: FP10SH)**	Turns ON while data is not send during the serial data communicating. (by the **F144 (TRNS)** instruction) Turns OFF while data is being sent during the serial data communicating. (by the **F144 (TRNS)** instruction)
R903A	————————	Not used
R903B	————————	Not used
R903C	————————	Not used
R903D	————————	Not used
R903E	————————	Not used
R903F	————————	Not used
R9050	**MEWNET–W/–P link transmission error flag [W/P LINK 1]**	When using MEWNET-W link unit or MEWNET–P link unit: – turns ON when transmission error occurs at link 1. – turns ON when there is an error in the link area settings.
R9051	**MEWNET–W/–P link transmission error flag [W/P LINK 2]**	When using MEWNET-W link unit or MEWNET–P link unit: – turns ON when transmission error occurs at link 2. – turns ON when there is an error in the link area settings.
R9052	**MEWNET–W/–P link transmission error flag [W/P LINK 3]**	When using MEWNET-W link unit or MEWNET–P link unit: – turns ON when transmission error occurs at link 3. – turns ON when there is an error in the link area settings.
R9053	**MEWNET–W/–P link transmission error flag [W/P LINK 4] (Available PLC: FP10SH)**	When using MEWNET-W link unit or MEWNET–P link unit: – turns ON when transmission error occurs at link 4. – turns ON when there is an error in the link area settings.
R9054	**MEWNET–W/–P link transmission error flag [W/P LINK 5] (Available PLC: FP10SH)**	When using MEWNET-W link unit or MEWNET–P link unit: – turns ON when transmission error occurs at link 5. – turns ON when there is an error in the link area settings.
R9055	**MEWNET–H link transmission error flag [H LINK 1] (FP3 CPU Ver.4.3 or later)**	When using MEWNET–H link unit: – turns ON when trannsmission error occurs at H link 1. – turns ON when there is an error in the link area settings.
R9056	**MEWNET–H link transmission error flag [H LINK 2] (FP3 CPU Ver.4.3 or later)**	When using MEWNET–H link unit: – turns ON when trannsmission error occurs at H link 2. – turns ON when there is an error in the link area settings.
R9057	**MEWNET–H link transmission error flag [H LINK 3] (FP3 CPU Ver.4.3 or later)**	When using MEWNET–H link unit: – turns ON when trannsmission error occurs at H link 3. – turns ON when there is an error in the link area settings.

Address	Name	Description
R9058	**Remote I/O transmission error flag (master 1)**	When using remote I/O system (MEWNET-F): – turns ON when transmission error occurs on master 1. – turns ON when there is an error in the settings.
R9059	**Remote I/O transmission error flag (master 2)**	When using remote I/O system (MEWNET-F): – turns ON when transmission error occurs on master 2. – turns ON when there is an error in the settings.
R905A	**Remote I/O transmission error flag (master 3)**	When using remote I/O system (MEWNET-F): – turns ON when transmission error occurs on master 3. – turns ON when there is an error in the settings.
R905B	**Remote I/O transmission error flag (master 4)**	When using remote I/O system (MEWNET-F): – turns ON when transmission error occurs on master 4. – turns ON when there is an error in the settings.
R905C	————————	Not used
R905D	————————	Not used
R905E	————————	Not used
R905F	————————	Not used

Address	Name		Description
R9060	**MEWNET−W/ −P PC link transmission assurance relay [for PC link 0(W/P)]**	**Unit No.1**	Turns ON when unit No. 1 is communicating properly in the PC link mode. Turns OFF when operation is stopped, when an error is occurring, or when not in the PC link mode.
R9061		**Unit No.2**	Turns ON when unit No. 2 is communicating properly in the PC link mode. Turns OFF when operation is stopped, when an error is occurring, or when not in the PC link mode.
R9062		**Unit No.3**	Turns ON when unit No. 3 is communicating properly in the PC link mode. Turns OFF when operation is stopped, when an error is occurring, or when not in the PC link mode.
R9063		**Unit No.4**	Turns ON when unit No. 4 is communicating properly in the PC link mode. Turns OFF when operation is stopped, when an error is occurring, or when not in the PC link mode.
R9064		**Unit No.5**	Turns ON when unit No. 5 is communicating properly in the PC link mode. Turns OFF when operation is stopped, when an error is occurring, or when not in the PC link mode.
R9065		**Unit No.6**	Turns ON when unit No. 6 is communicating properly in the PC link mode. Turns OFF when operation is stopped, when an error is occurring, or when not in the PC link mode.
R9066		**Unit No.7**	Turns ON when unit No. 7 is communicating properly in the PC link mode. Turns OFF when operation is stopped, when an error is occurring, or when not in the PC link mode.
R9067		**Unit No.8**	Turns ON when unit No. 8 is communicating properly in the PC link mode. Turns OFF when operation is stopped, when an error is occurring, or when not in the PC link mode.
R9068		**Unit No.9**	Turns ON when unit No. 9 is communicating properly in the PC link mode. Turns OFF when operation is stopped, when an error is occurring, or when not in the PC link mode.
R9069		**Unit No.10**	Turns ON when unit No. 10 is communicating properly in the PC link mode. Turns OFF when operation is stopped, when an error is occurring, or when not in the PC link mode.
R906A		**Unit No.11**	Turns ON when unit No. 11 is communicating properly in the PC link mode. Turns OFF when operation is stopped, when an error is occurring, or when not in the PC link mode.

Address	Name		Description
R906B	**MEWNET–W/ –P PC link transmission assurance relay [for PC link 0(W/P)]**	**Unit No.12**	Turns ON when unit No. 12 is communicating properly in the PC link mode. Turns OFF when operation is stopped, when an error is occurring, or when not in the PC link mode.
R906C		**Unit No.13**	Turns ON when unit No. 13 is communicating properly in the PC link mode. Turns OFF when operation is stopped, when an error is occurring, or when not in the PC link mode.
R906D		**Unit No.14**	Turns ON when unit No. 14 is communicating properly in the PC link mode. Turns OFF when operation is stopped, when an error is occurring, or when not in the PC link mode.
R906E		**Unit No.15**	Turns ON when unit No. 15 is communicating properly in the PC link mode. Turns OFF when operation is stopped, when an error is occurring, or when not in the PC link mode.
R906F		**Unit No.16**	Turns ON when unit No. 16 is communicating properly in the PC link mode. Turns OFF when operation is stopped, when an error is occurring, or when not in the PC link mode.

Address	Name		Description
R9070	MEWNET–W/–P PC link operation mode relay [for PC link 0(W/P)]	Unit No.1	Turns ON when unit No. 1 is in the RUN mode. Turns OFF when unit No. 1 is in the PROG. mode.
R9071		Unit No.2	Turns ON when unit No. 2 is in the RUN mode. Turns OFF when unit No. 2 is in the PROG. mode.
R9072		Unit No.3	Turns ON when unit No. 3 is in the RUN mode. Turns OFF when unit No. 3 is in the PROG. mode.
R9073		Unit No.4	Turns ON when unit No. 4 is in the RUN mode. Turns OFF when unit No. 4 is in the PROG. mode.
R9074		Unit No.5	Turns ON when unit No. 5 is in the RUN mode. Turns OFF when unit No. 5 is in the PROG. mode.
R9075		Unit No.6	Turns ON when unit No. 6 is in the RUN mode. Turns OFF when unit No. 6 is in the PROG. mode.
R9076		Unit No.7	Turns ON when unit No. 7 is in the RUN mode. Turns OFF when unit No. 7 is in the PROG. mode.
R9077		Unit No.8	Turns ON when unit No. 8 is in the RUN mode. Turns OFF when unit No. 8 is in the PROG. mode.
R9078		Unit No.9	Turns ON when unit No. 9 is in the RUN mode. Turns OFF when unit No. 9 is in the PROG. mode.
R9079		Unit No.10	Turns ON when unit No. 10 is in the RUN mode. Turns OFF when unit No. 10 is in the PROG. mode.
R907A		Unit No.11	Turns ON when unit No. 11 is in the RUN mode. Turns OFF when unit No. 11 is in the PROG. mode.
R907B		Unit No.12	Turns ON when unit No. 12 is in the RUN mode. Turns OFF when unit No. 12 is in the PROG. mode.
R907C		Unit No.13	Turns ON when unit No. 13 is in the RUN mode. Turns OFF when unit No. 13 is in the PROG. mode.
R907D		Unit No.14	Turns ON when unit No. 14 is in the RUN mode. Turns OFF when unit No. 14 is in the PROG. mode.
R907E		Unit No.15	Turns ON when unit No. 15 is in the RUN mode. Turns OFF when unit No. 15 is in the PROG. mode.
R907F		Unit No.16	Turns ON when unit No. 16 is in the RUN mode. Turns OFF when unit No. 16 is in the PROG. mode.
R9080	MEWNET–W/–P PC link transmission assurance relay [for PC link 1 (W/P)]	Unit No.1	Turns ON when unit No. 1 is communicating probably in the PC link mode. Turns OFF when operation is stopped, when an error is occurring, or when not in the PC link mode.
R9081		Unit No.2	Turns ON when unit No. 2 is communicating probably in the PC link mode. Turns OFF when operation is stopped, when an error is occurring, or when not in the PC link mode.
R9082		Unit No.3	Turns ON when unit No. 3 is communicating probably in the PC link mode. Turns OFF when operation is stopped, when an error is occurring, or when not in the PC link mode.

Address	Name		Description
R9083	**MEWNET–W/ –P PC link transmission assurance relay [for PC link 1 (W/P)]**	**Unit No.4**	Turns ON when unit No. 4 is communicating probably in the PC link mode. Turns OFF when operation is stopped, when an error is occurring, or when not in the PC link mode.
R9084		**Unit No.5**	Turns ON when unit No. 5 is communicating probably in the PC link mode. Turns OFF when operation is stopped, when an error is occurring, or when not in the PC link mode.
R9085		**Unit No.6**	Turns ON when unit No. 6 is communicating probably in the PC link mode. Turns OFF when operation is stopped, when an error is occurring, or when not in the PC link mode.
R9086		**Unit No.7**	Turns ON when unit No. 7 is communicating probably in the PC link mode. Turns OFF when operation is stopped, when an error is occurring, or when not in the PC link mode.
R9087		**Unit No.8**	Turns ON when unit No. 8 is communicating probably in the PC link mode. Turns OFF when operation is stopped, when an error is occurring, or when not in the PC link mode.
R9088		**Unit No.9**	Turns ON when unit No. 9 is communicating probably in the PC link mode. Turns OFF when operation is stopped, when an error is occurring, or when not in the PC link mode.
R9089		**Unit No.10**	Turns ON when unit No. 10 is communicating probably in the PC link mode. Turns OFF when operation is stopped, when an error is occurring, or when not in the PC link mode.
R908A		**Unit No.11**	Turns ON when unit No. 11 is communicating probably in the PC link mode. Turns OFF when operation is stopped, when an error is occurring, or when not in the PC link mode.
R908B		**Unit No.12**	Turns ON when unit No. 12 is communicating probably in the PC link mode. Turns OFF when operation is stopped, when an error is occurring, or when not in the PC link mode.
R908C		**Unit No.13**	Turns ON when unit No. 13 is communicating probably in the PC link mode. Turns OFF when operation is stopped, when an error is occurring, or when not in the PC link mode.
R908D		**Unit No.14**	Turns ON when unit No. 14 is communicating probably in the PC link mode. Turns OFF when operation is stopped, when an error is occurring, or when not in the PC link mode.

Address	Name		Description
R908E	MEWNET–W/–P PC link transmission assurance relay [for PC link 1 (W/P)]	Unit No.15	Turns ON when unit No. 15 is communicating probably in the PC link mode. Turns OFF when operation is stopped, when an error is occurring, or when not in the PC link mode.
R908F		Unit No.16	Turns ON when unit No. 16 is communicating probably in the PC link mode. Turns OFF when operation is stopped, when an error is occurring, or when not in the PC link mode.
R9090	MEWNET-W/–P PC link operation mode relay [for PC link 1 (W/P)]	Unit No.1	Turns ON when unit No. 1 is in the RUN mode. Turns OFF when unit No. 1 is in the PROG. mode.
R9091		Unit No.2	Turns ON when unit No. 2 is in the RUN mode. Turns OFF when unit No. 2 is in the PROG. mode.
R9092		Unit No.3	Turns ON when unit No. 3 is in the RUN mode. Turns OFF when unit No. 3 is in the PROG. mode.
R9093		Unit No.4	Turns ON when unit No. 4 is in the RUN mode. Turns OFF when unit No. 4 is in the PROG. mode.
R9094		Unit No.5	Turns ON when unit No. 5 is in the RUN mode. Turns OFF when unit No. 5 is in the PROG. mode.
R9095		Unit No.6	Turns ON when unit No. 6 is in the RUN mode. Turns OFF when unit No. 6 is in the PROG. mode.
R9096		Unit No.7	Turns ON when unit No. 7 is in the RUN mode. Turns OFF when unit No. 7 is in the PROG. mode.
R9097		Unit No.8	Turns ON when unit No. 8 is in the RUN mode. Turns OFF when unit No. 8 is in the PROG. mode.
R9098		Unit No.9	Turns ON when unit No. 9 is in the RUN mode. Turns OFF when unit No. 9 is in the PROG. mode.
R9099		Unit No.10	Turns ON when unit No. 10 is in the RUN mode. Turns OFF when unit No. 10 is in the PROG. mode.
R909A		Unit No.11	Turns ON when unit No. 11 is in the RUN mode. Turns OFF when unit No.11 is in the PROG. mode.
R909B		Unit No.12	Turns ON when unit No. 12 is in the RUN mode. Turns OFF when unit No. 12 is in the PROG. mode.
R909C		Unit No.13	Turns ON when unit No. 13 is in the RUN mode. Turns OFF when unit No. 13 is in the PROG. mode.
R909D		Unit No.14	Turns ON when unit No. 14 is in the RUN mode. Turns OFF when unit No. 14 is in the PROG. mode.
R909E		Unit No.15	Turns ON when unit No. 15 is in the RUN mode. Turns OFF when unit No. 15 is in the PROG. mode.
R909F		Unit No.16	Turns ON when unit No. 16 is in the RUN mode. Turns OFF when unit No. 16 is in the PROG. mode.

Address	Name	Description
R9100	**IC memory card installation flag (Available PLC: FP10SH)**	Monitors whether the IC memory card is installed or not: – ON: IC memory card is installed. – OFF: IC memory card is not installed.
R9101	**IC memory card backup battery flag 1 (* Note) (Available PLC: FP10SH)**	Monitors the voltage drop condition for the IC memory card as: – ON: Data in the IC memory card cannot be guaranteed. – OFF: Data in the IC memory card can be maintained.
R9102	**IC memory card backup battery flag 2 (* Note) (Available PLC: FP10SH)**	Monitors the voltage drop condition for the IC memory card as: – ON: Battery replacement is required. – OFF: Battery replacement is not required.
R9103	**IC memory card protect switch flag (Available PLC: FP10SH)**	Monitors the protective condition of the IC memory card as: – ON: Switch is not in the write–protected (WP) position – OFF: Switch is in the write–protected (WP) position
R9104	**IC memory card access switch flag (Available PLC: FP10SH)**	Monitors the condition of the IC memory card access enable switch as: – ON: The access enable switch is in the ON position (Access enabled). – OFF: The access enable switch is in the OFF position (Access disabled).
R9105 through R910F	————————	Not used

☞ **Note**

The IC memory card backup battery condition can be judged using internal relays R9101 and R9102 as follows:

R9101	R9102	IC memory card condition
OFF	**OFF**	Not battery replacement required.
OFF	**ON**	Replace backup battery. The data in the IC memory card is maintained.
ON	**ON**	The IC memory card has lost its data. Replace backup battery.

Appendix E

Table of Special Data Registers

The special data registers are one-word (16-bit) memory areas which store specific information. With the exception of registers for which “Writing is possible” is indicated in the “Description” column, these registers cannot be written to.

Address FP3	Address FP10SH	Name	Description
DT9000	DT90000	Self-diagnostic error code	The self-diagnostic error code is stored here when a self-diagnostic error occurs. Monitor the error code using decimal display. See Appendix F.
DT9001	DT90001	———————	Not used
DT9002	DT90002	Erroneous MEWNET–TR master unit (slot No. 0 to 15)	The slot number, where an erroneous unit is installed, can be monitored here. “1” (ON) is set in the bit position corresponding to the slot number when an erroneous MEWNET–TR master unit is detected. **Bit position** 15 . . 12 11 . . 8 7 . . 4 3 . . 0 **Slot number** 15 . . 12 11 . . 8 7 . . 4 3 . . 0 DT9002/DT90002
DT9003	DT90003	Erroneous MEWNET–TR master unit (slot No. 16 to 31)	**Bit position** 15 . . 12 11 . . 8 7 . . 4 3 . . 0 **Slot number** 31 . . 28 27 . . 24 23 . . 20 19 . . 16 DT9003/DT90003 1: error 0: normal
DT9004	DT90004	———————	Not used
DT9005	DT90005	———————	Not used
DT9006	DT90006	Abnormal intelligent unit (slot No. 0 to 15)	When an error condition is detected in an intelligent unit, the bit corresponding to the slot of the unit will be set to ON. Monitor using binary display. **Bit position** 15 . . 12 11 . . 8 7 . . 4 3 . . 0 **Slot number** 15 . . 12 11 . . 8 7 . . 4 3 . . 0 DT9006/DT90006
DT9007	DT90007	Abnormal intelligent unit (slot No. 16 to 31)	**Bit position** 15 . . 12 11 . . 8 7 . . 4 3 . . 0 **Slot number** 31 . . 28 27 . . 24 23 . . 20 19 . . 16 DT9007/DT90007 1: abnormal intelligent unit 0: normal intelliget unit
DT9008	DT90008	———————	Not used
DT9009	DT90009	———————	Not used
DT9010	DT90010	I/O verify error unit (slot No. 0 to 15)	When the state of installation of an I/O unit has changed since the power was turned ON, the bit corresponding to the slot of the unit will be set to ON. Monitor using binary display. **Bit position** 15 . . 12 11 . . 8 7 . . 4 3 . . 0 **Slot number** 15 . . 12 11 . . 8 7 . . 4 3 . . 0 DT9010/DT90010
DT9011	DT90011	I/O verify error unit (slot No. 16 to 31)	**Bit position** 15 . . 12 11 . . 8 7 . . 4 3 . . 0 **Slot number** 31 . . 28 27 . . 24 23 . . 20 19 . . 16 DT9011/DT90011 1: error 0: normal

Address		Name	Description
FP3	FP10SH		
DT9012	**DT90012**	————	Not used
DT9013	**DT90013**	————	Not used
DT9014	**DT90014**	Auxiliary register for operation	One shift-out hexadecimal digit is stored in bit positions 0 to 3 when an **F105 (BSR)**/**P105 (PBSR)** or **F106 (BSL)**/**P106 (PBSL)** instruction is executed.
DT9015 **DT9016**	**DT90015** **DT90016**	Auxiliary register for operation	The divided remainder (16-bit) is stored in DT9015/DT90015 when an **F32 (%)**/**P32 (P%)** or **F52 (B%)**/**P52 (PB%)** instruction is executed. The divided remainder (32-bit) is stored DT9015 and DT9016/DT90015 and DT90016 when an **F33 (D%)**/**P33 (PD%)** or **F53 (DB%)**/**P53 (PDB%)** instruction is executed.
DT9017	**DT90017**	Operation error address (hold)	After commencing operation, the address where the first operation error occurred is stored. Monitor the address using decimal display.
DT9018	**DT90018**	Operation error address (non-hold)	The address where a operation error occurred is stored. Each time an error occurs, the new address overwrites the previous address. At the beginning of scan, the address is 0. Monitor the address using decimal display.
DT9019	**DT90019**	2.5 ms ring counter	The data stored here is increased by one every 2.5 ms. (H0 to HFFFF) Difference between the values of the two points (absolute value) × 2.5 ms = Elapsed time between the two points.
DT9020	————	Maximum value of program (for FP3)	The last address of sequence program area set in system register 0 is stored.
————	**DT90020**	Display of program capacity (for FP10SH)	The program capacity is stored in decimal. **<Example>** K30: approx. 30 K steps K60: approx. 60 K steps (with memory expansion)
DT9021 **(* Note)**	**DT90021** **(* Note)**	Maximum value of file register	The maximum (last) address of the file registers available are stored in: – FP3: DT9021 – FP10SH: DT90021

☞ **Note**

Used by the system.

<table>
<tr><th colspan="2">Address</th><th rowspan="2">Name</th><th rowspan="2" colspan="2">Description</th></tr>
<tr><th>FP3</th><th>FP10SH</th></tr>
<tr><td>DT9022</td><td>DT90022</td><td>Scan time (current value)</td><td>The current scan time is stored here. Scan time is calculated using the formula:
Scan time (ms) = stored data (decimal) × 0.1
<Example>
K50 indicates 5 ms.</td><td rowspan="3">Scan time display is only possible in RUN mode, and shows the operation cycle time. The maximum and minimum values are cleared when each the mode is switched between RUN mode and PROG. mode.</td></tr>
<tr><td>DT9023</td><td>DT90023</td><td>Scan time (minimum value)</td><td>The minimum scan time is stored here. Scan time is calculated using the formula:
Scan time (ms) = stored data (decimal) × 0.1
<Example>
K50 indicates 5 ms.</td></tr>
<tr><td>DT9024</td><td>DT90024</td><td>Scan time (maximum value)</td><td>The maximum scan time is stored here. Scan time is calculated using the formula:
Scan time (ms) = stored data (decimal) × 0.1
<Example>
K125 indicates 12.5 ms.</td></tr>
<tr><td>DT9025
(* Note)</td><td>DT90025
(* Note)</td><td>Mask condition monitoring register for interrupt unit initiated interrupts
(INT 0 to INT 15)</td><td colspan="2">The mask conditions of interrupt unit initiated interrupts using ICTL instruction can be monitored here. Monitor using binary display.
<table>
<tr><td>Bit position</td><td>15 . . 12</td><td>11 . . 8</td><td>7 . . 4</td><td>3 . . 0</td></tr>
<tr><td>INT program</td><td>15 . . 12</td><td>11 . . 8</td><td>7 . . 4</td><td>3 . . 0</td></tr>
<tr><td>DT9025/DT90025</td><td></td><td></td><td></td><td></td></tr>
</table>
0: interrupt disabled (masked)
1: interrupt enabled (unmasked)</td></tr>
<tr><td>DT9026</td><td>DT90026</td><td>Mask condition monitoring register for intelligent unit initiated interrupts
(INT 16 to INT 32)</td><td colspan="2">The mask conditions of intelligent unit initiated interrupts using ICTL instruction can be monitored here. Monitor using binary display.
<table>
<tr><td>Bit position</td><td>15 . . 12</td><td>11 . . 8</td><td>7 . . 4</td><td>3 . . 0</td></tr>
<tr><td>INT program</td><td>———</td><td>———</td><td>23 . . 20</td><td>19 . . 16</td></tr>
<tr><td>DT9026/DT90026</td><td></td><td></td><td></td><td></td></tr>
</table>
0: interrupt disabled (masked)
1: interrupt enabled (unmasked)</td></tr>
<tr><td>DT9027
(* Note)</td><td>DT90027
(* Note)</td><td>Periodical interrupt interval (INT24)</td><td colspan="2">The value set by ICTL instruction is stored.
– K0: periodical interrupt is not used
– K1 to K3000: 10 ms to 30 s</td></tr>
<tr><td>DT9028
(* Note)</td><td>DT90028
(* Note)</td><td>Sample trace interval</td><td colspan="2">The value registered using NPST-GR is stored.
– K0: sampling triggered by F155 (SMPL)/P155 (PSMPL) instruction
– K1 to K3000 (× 10 ms): 10 ms to 30 s</td></tr>
</table>

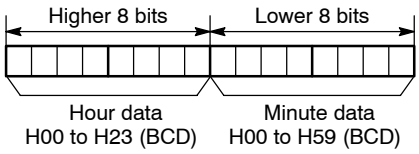
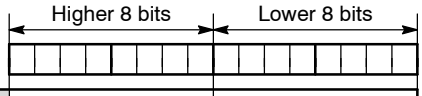
☞ **Note**

Used by the system.

Address		Name	Description
FP3	**FP10SH**		
DT9029 (* Note)	**DT90029 (* Note)**	Break address	The address (K constant) of a break in a test run is stored.
DT9030 (* Note)	**DT90030 (* Note)**	Message 0	The contents of the specified message are stored in these special data registers when an **F149 (MSG)**/**P149 (PMSG)** instruction is executed.
DT9031 (* Note)	**DT90031 (* Note)**	Message 1	
DT9032 (* Note)	**DT90032 (* Note)**	Message 2	
DT9033 (* Note)	**DT90033 (* Note)**	Message 3	
DT9034 (* Note)	**DT90034 (* Note)**	Message 4	
DT9035 (* Note)	**DT90035 (* Note)**	Message 5	
DT9036	**DT90036**	**F152 (RMRD)**/**P152 (PRMRD)** and **F153 (RMWT)**/**P153 (PRMWT)** instructions end code	The error code is stored here if an **F152 (RMRD)**/**P152 (PRMRD)** or **F153 (RMWT)**/**P153 (PRMWT)** instruction was executed abnormally. When the instruction was successfully executed “0” is stored. – Other than K0: error code is stored. Refer to the description for the **F152 (RMRD)**/**P152 (PRMRD)** and **F153 (RMWT)**/**P153 (PRMWT)** instructions and the MEWNET-F (REMOTE I/O) SYSTEM manual.
		Abnormal unit display	If an abnormal unit is installed to the backplane, the slot number of that unit will be stored. Monitor using decimal display.
DT9037	**DT90037**	Work 1 for **F96 (SRC)**/**P96 (PSRC)** instructions	The number of found data is stored here when an **F96 (SRC)**/**P96 (PSRC)** instruction is executed.
DT9038	**DT90038**	Work 2 for **F96 (SRC)**/**P96 (PSRC)** instructions	The data position, found in the first place counting from the first 16-bit area, is stored here when an **F96 (SRC)**/**P96 (PSRC)** instruction is executed.
DT9039	**DT90039**	**F145 (SEND)**/**P145 (PSEND)** and **F146 (RECV)**/**P146 (PRECV)** instructions end code	The error code is stored here if an **F145 (SEND)**/**P145 (PSEND)** or **F146 (RECV)**/**P146 (PRECV)** instruction was executed abnormally. – K0: instruction was successfully executed. – Other than K0: error code is stored. Refer to the description for the **F145 (SEND)**/**P145 (PSEND)** and **F146 (RECV)**/**P146 (PRECV)** instructions and the manual of MEWNET link system.

☞ **Note**

Used by the system.

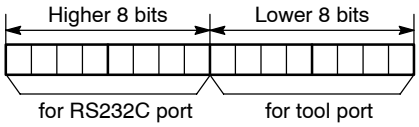
Address		Name	Description
FP3	**FP10SH**		
DT9053	**DT90053**	Clock/calendar monitor (hour/minute)	Hour and minute data of the clock/calendar are stored here. This data is read-only data; it cannot be overwritten. 
DT9054	**DT90054**	Clock/calendar monitor and setting (minute/second)	The year, month, day, hour, minute, second, and day-of-the-week data for the calendar timer is stored. The built-in calendar timer will operate correctly through the year 2099 and supports leap years. The calendar timer can be set (the time set) by writing a value using a programming tool or a program that uses the **F0 (MV)** transfer instruction. 
DT9055	**DT90055**	Clock/calendar monitor and setting (day/hour)	
DT9056	**DT90056**	Clock/calendar monitor and setting (year/month)	
DT9057	**DT90057**	Clock/calendar monitor and setting (day-of-the-week)	

DT9054/ DT90054	Minute H00 to H59 (BCD)	Second H00 to H59 (BCD)
DT9055/ DT90055	Day H01 to H31 (BCD)	Hour H00 to H23 (BCD)
DT9056/ DT90056	Year H00 to H99 (BCD)	Month H01 to H12 (BCD)
DT9057/ DT90057	————	Day-of-the-week H00 to H06 (BCD)

Address		Name	Description
FP3	FP10SH		
DT9058 (* Note)	**DT90058 (* Note)**	Clock/calendar time setting and 30s correction	The clock/calendar is adjusted as follows. **When setting the clock/calendar by program that uses F0 (MV) instructions** By setting the the highest bit of DT9058/DT90058 to 1, the time becomes that written to DT9054 to DT9057/DT90054 to DT90057 by **F0 (MV)** instruction. After the time is set, DT9058/DT90058 is cleared to 0. (Cannot be performed with any instruction other than **F0 (MV)** instruction.) **<EXAMPLE>** Set the time to 12:00:00 on the 5th day when the X0 turns ON. X0 (DF) > 1 1 > [F0 MV, H 0, DT9054] . . Inputs 0 minutes and 0 seconds [F0 MV, H 512, DT9055] . . Inputs 12th hour 5th day [F0 MV, H8000, DT9058] . . Sets the time ☞ **Note** **If you changed the values of DT9054 to DT9057/DT90054 to DT90057 with the data monitor functions of NPST-GR software or FP programmer II, the time will be set when the new values are written. Therefore, it is unnecessary to write to DT9058/DT90058.** **When the correcting times less than 30 seconds** By setting the lowest bit of DT9058/DT90058 to 1, the value will be moved up or down and become exactly 0 seconds. After the correction is completed, DT9058/DT90058 is cleared to 0. **<EXAMPLE>** Correct to 0 seconds with X0 turns ON X0 (DF) > 1 1 > [F0 MV, H 0, DT9058] Correct to 0 second. At the time of correction, if between 0 and 29 seconds, it will be moved down, and if the between 30 and 59 seconds, it will be moved up. In the example above, if the time was 5 minutes 29 seconds, it will become 5 minutes 0 second; and, if the time was 5 minutes 35 seconds, it will become 6 minutes 0 second.

☞ **Note**

Used by the system.

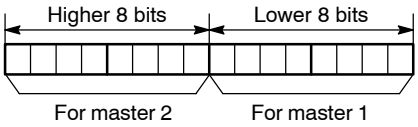
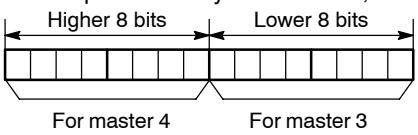
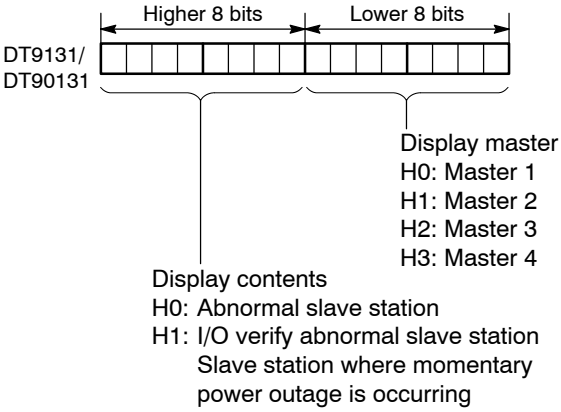
<table>
<tr><th colspan="2">Address</th><th rowspan="2">Name</th><th rowspan="2">Description</th></tr>
<tr><th>FP3</th><th>FP10SH</th></tr>
<tr><td>DT9059
(* Note)</td><td>DT90059
(* Note)</td><td>Communication error code</td><td>The error code (decimal) is stored when communication error occurs.
 
</td></tr>
<tr><td>DT9060</td><td>DT90060</td><td>Step ladder process (0 to 15)</td><td rowspan="17">Indicates the startup condition of the step ladder process.
When the process starts up, the bit corresponding to the process number turns ON.
Monitor using binary display.
<Example>
<table>
<tr><td>Bit position</td><td>15 . . 12</td><td>11 . . 8</td><td>7 . . 4</td><td>3 . . 0</td></tr>
<tr><td>Process number</td><td>15 . . 12</td><td>11 . . 8</td><td>7 . . 4</td><td>3 . . 0</td></tr>
<tr><td>DT9060/DT90060</td><td>0 0 0 0</td><td>0 0 0 0</td><td>0 0 0 0</td><td>0 0 0 1</td></tr>
</table>
0: not-executing
1: executing
Since bit position 0 of DT9060/DT90060 is “1”, step ladder process 0 is executing.
A programming tool can be used to write data.</td></tr>
<tr><td>DT9061</td><td>DT90061</td><td>Step ladder process (16 to 31)</td></tr>
<tr><td>DT9062</td><td>DT90062</td><td>Step ladder process (32 to 47)</td></tr>
<tr><td>DT9063</td><td>DT90063</td><td>Step ladder process (48 to 63)</td></tr>
<tr><td>DT9064</td><td>DT90064</td><td>Step ladder process (64 to 79)</td></tr>
<tr><td>DT9065</td><td>DT90065</td><td>Step ladder process (80 to 95)</td></tr>
<tr><td>DT9066</td><td>DT90066</td><td>Step ladder process (96 to 111)</td></tr>
<tr><td>DT9067</td><td>DT90067</td><td>Step ladder process (112 to 127)</td></tr>
<tr><td>DT9068</td><td>DT90068</td><td>Step ladder process (128 to 143)</td></tr>
<tr><td>DT9069</td><td>DT90069</td><td>Step ladder process (144 to 159)</td></tr>
<tr><td>DT9070</td><td>DT90070</td><td>Step ladder process (160 to 175)</td></tr>
<tr><td>DT9071</td><td>DT90071</td><td>Step ladder process (176 to 191)</td></tr>
<tr><td>DT9072</td><td>DT90072</td><td>Step ladder process (192 to 207)</td></tr>
<tr><td>DT9073</td><td>DT90073</td><td>Step ladder process (208 to 223)</td></tr>
<tr><td>DT9074</td><td>DT90074</td><td>Step ladder process (224 to 239)</td></tr>
<tr><td>DT9075</td><td>DT90075</td><td>Step ladder process (240 to 255)</td></tr>
<tr><td>DT9076</td><td>DT90076</td><td>Step ladder process (256 to 271)</td></tr>
<tr><td>DT9077</td><td>DT90077</td><td>Step ladder process (272 to 287)</td></tr>
</table>

☞ **Note**

Used by the system.

Address		Name	Description
FP3	FP10SH		
DT9078	DT90078	Step ladder process (288 to 303)	Indicates the startup condition of the step ladder process. When the process starts up, the bit corresponding to the process number turns ON. Monitor using binary display. **<Example>** **Bit position** 15 . . 12 11 . . 8 7 . . 4 3 . . 0 **Process number** 335 . .332 331 . .328 327 . .324 323 . .320 **DT9080/DT90080** 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 1 0: not-executing, 1: executing Since bit position 0 of DT9080/DT90080 is “1”, step ladder process 320 is executing. A programming tool can be used to write data.
DT9079	DT90079	Step ladder process (304 to 319)	
DT9080	DT90080	Step ladder process (320 to 335)	
DT9081	DT90081	Step ladder process (336 to 351)	
DT9082	DT90082	Step ladder process (352 to 367)	
DT9083	DT90083	Step ladder process (368 to 383)	
DT9084	DT90084	Step ladder process (384 to 399)	
DT9085	DT90085	Step ladder process (400 to 415)	
DT9086	DT90086	Step ladder process (416 to 431)	
DT9087	DT90087	Step ladder process (432 to 447)	
DT9088	DT90088	Step ladder process (448 to 463)	
DT9089	DT90089	Step ladder process (464 to 479)	
DT9090	DT90090	Step ladder process (480 to 495)	
DT9091	DT90091	Step ladder process (496 to 511)	
DT9092	DT90092	Step ladder process (512 to 527)	
DT9093	DT90093	Step ladder process (528 to 543)	
DT9094	DT90094	Step ladder process (544 to 559)	
DT9095	DT90095	Step ladder process (560 to 575)	
DT9096	DT90096	Step ladder process (576 to 591)	
DT9097	DT90097	Step ladder process (592 to 607)	
DT9098	DT90098	Step ladder process (608 to 623)	
DT9099	DT90099	Step ladder process (624 to 639)	

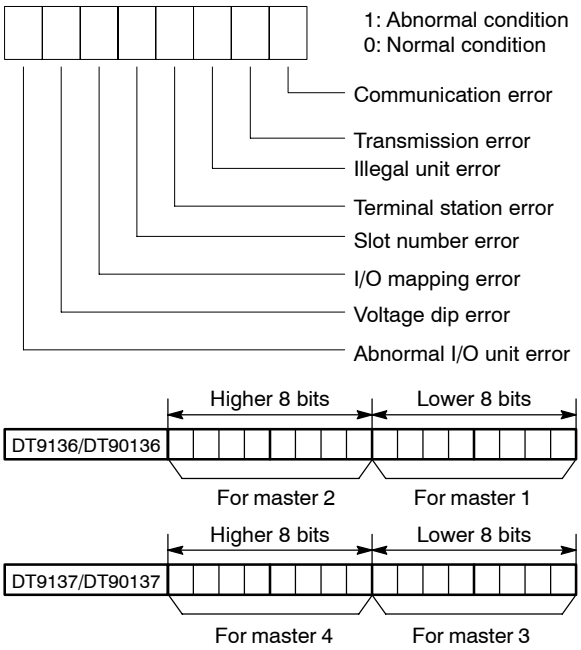
Address		Name	Description
FP3	FP10SH		
DT9100	DT90100	Step ladder process (640 to 655)	Indicates the startup condition of the step ladder process. When the process starts up, the bit corresponding to the process number turns ON. Monitor using binary display. **<Example>** **Bit position** 15 . . 12 11 . . 8 7 . . 4 3 . . 0 **Process number** 655 . .652 651 . .648 647 . .644 643 . .640 **DT9100/DT90100** 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 1 0: not-executing, 1: executing Since bit position 0 of DT9100/DT90100 is “1”, step ladder process 640 is executing. A programming tool can be used to write data.
DT9101	DT90101	Step ladder process (656 to 671)	
DT9102	DT90102	Step ladder process (672 to 687)	
DT9103	DT90103	Step ladder process (688 to 703)	
DT9104	DT90104	Step ladder process (704 to 719)	
DT9105	DT90105	Step ladder process (720 to 735)	
DT9106	DT90106	Step ladder process (736 to 751)	
DT9107	DT90107	Step ladder process (752 to 767)	
DT9108	DT90108	Step ladder process (768 to 783)	
DT9109	DT90109	Step ladder process (784 to 799)	
DT9110	DT90110	Step ladder process (800 to 815)	
DT9111	DT90111	Step ladder process (816 to 831)	
DT9112	DT90112	Step ladder process (832 to 847)	
DT9113	DT90113	Step ladder process (848 to 863)	
DT9114	DT90114	Step ladder process (864 to 879)	
DT9115	DT90115	Step ladder process (880 to 895)	
DT9116	DT90116	Step ladder process (896 to 911)	
DT9117	DT90117	Step ladder process (912 to 927)	
DT9118	DT90118	Step ladder process (928 to 943)	
DT9119	DT90119	Step ladder process (944 to 959)	
DT9120	DT90120	Step ladder process (960 to 975)	
DT9121	DT90121	Step ladder process (976 to 991)	
DT9122	DT90122	Step ladder process (992 to 999) (Higher byte: not used)	

Address		Name	Description
FP3	FP10SH		
DT9123	DT90123	————	Not used
DT9124	DT90124	————	Not used
DT9125	DT90125	————	Not used
DT9126 (* Note)	DT90126 (* Note)	Forced ON/OFF operating station monitor	This displays the number of a unit that has executed forced ON/OFF operation.
DT9127 (* Note)	DT90127 (* Note)	MEWNET-F system remote I/O service time	The number of times, which MEWNET−F remote I/O service was performed by each master, is stored. 
DT9128 (* Note)	DT90128 (* Note)		The number of times, which MEWNET−F remote I/O service was performed by each master, is stored. 
DT9129	DT90129	————	Not used
DT9130	DT90130	————	Not used
DT9131	DT90131	MEWNET-F (remote I/O) slave stations abnormality checking (for selecting the display contents and master of DT9132 to DT9135/DT90132 to DT90135)	The contents displayed by DT9132 to DT9135/ DT90132 to DT90135 will change depending on the contents of stored in DT9131/DT90131. Use the programming tools to write the settings for what you want to display (this can also be done with the **F0 (MV)** move instruction). Set the code specifying the display contents (H0 or H1) in the higher 8 bits and set the code specifying the display master (H0 to H3) in the lower 8 bits. 

☞ **Note**

Used by the system.

Address		Name	Description
FP3	**FP10SH**		
DT9132 **DT9133**	**DT90132** **DT90133**	MEWNET-F (remote I/O) error slave station number - current condition (when DT9131/DT90131 is H0, H1, H2 or H3)	The bit corresponding to the station number of the MEWNET-F where an error is occurring is set to ON. Monitor using binary display. **Bit position** 15 . . 12 11 . . 8 7 . . 4 3 . . 0 **Slave station no.** 16 . . 13 12 . . 9 8 . . 5 4 . . 1 **DT9132/DT90132** **Bit position** 15 . . 12 11 . . 8 7 . . 4 3 . . 0 **Slave station no.** 32 . . 29 28 . . 25 24 . . 21 20 . . 17 **DT9133/DT90133** 1: Error slave station 0: Normal slave station
		MEWNET-F (remote I/O) I/O verify error slave station number (when DT9131/ DT90131 is H100, H101, H102 or H103)	When the installed condition of a MEWNET-F slave station set unit has changed since the power was turned ON, the bit corresponding to that slave station number will be set to ON. Monitor using binary display. **Bit position** 15 . . 12 11 . . 8 7 . . 4 3 . . 0 **Slave station no.** 16 . . 13 12 . . 9 8 . . 5 4 . . 1 **DT9132/DT90132** **Bit position** 15 . . 12 11 . . 8 7 . . 4 3 . . 0 **Slave station no.** 32 . . 29 28 . . 25 24 . . 21 20 . . 17 **DT9133/DT90133** 1: Error slave station 0: Normal slave station
DT9134 **DT9135**	**DT90134** **DT90135**	MEWNET-F (remote I/O) error slave station number - record (when DT9131/DT90131 is H0, H1, H2 or H3)	The bit corresponding to the slave station number of the MEWNET-F where an error is occurring will be set to ON. Monitor using binary display. **Bit position** 15 . . 12 11 . . 8 7 . . 4 3 . . 0 **Slave station no.** 16 . . 13 12 . . 9 8 . . 5 4 . . 1 **DT9134/DT90134** **Bit position** 15 . . 12 11 . . 8 7 . . 4 3 . . 0 **Slave station no.** 32 . . 29 28 . . 25 24 . . 21 20 . . 17 **DT9135/DT90135** 1: Error slave station 0: Normal slave station
		MEWNET-F (remote I/O) voltage dip slave station number (when DT9131/DT90131 is H100, H101, H102 or H103)	If a momentary power outage at an MEWNET-F slave station set, the bit corresponding to that slave station number will be set to ON. Monitor using binary display. **Bit position** 15 . . 12 11 . . 8 7 . . 4 3 . . 0 **Slave station no.** 16 . . 13 12 . . 9 8 . . 5 4 . . 1 **DT9134/DT90134** **Bit position** 15 . . 12 11 . . 8 7 . . 4 3 . . 0 **Slave station no.** 32 . . 29 28 . . 25 24 . . 21 20 . . 17 **DT9135/DT90135** 1: Error slave station 0: Normal slave station

Address		Name	Description
FP3	FP10SH		
DT9136 **DT9137**	**DT90136** **DT90137**	Error code of MEWNET-F (remote I/O) system	Displays the error conditions for 8 types of errors using 1 byte. 
DT9138	**DT90138**	———	Not used
DT9139	**DT90139**	———	Not used
DT9140 **(* Note 1)**	**DT90140** **(* Note 1)**	MEWNET-W/-P PC link status [PC link 0 (W/P)] **(* Note 2)**	The number of times the receiving operation is performed (counted using ring counter).
DT9141 **(* Note 1)**	**DT90141** **(* Note 1)**		The current interval between two receiving operations: value in the register × 2.5ms
DT9142 **(* Note 1)**	**DT90142** **(* Note 1)**		The minimum interval between two receiving operations: value in the register × 2.5ms
DT9143 **(* Note 1)**	**DT90143** **(* Note 1)**		The maximum interval between two receiving operations: value in the register × 2.5ms
DT9144 **(* Note 1)**	**DT90144** **(* Note 1)**		The number of times the sending operation is performed (counted using ring counter).
DT9145 **(* Note 1)**	**DT90145** **(* Note 1)**		The current interval between two sending operations: value in the register × 2.5ms
DT9146 **(* Note 1)**	**DT90146** **(* Note 1)**		The minimum interval between two sending operations: value in the register × 2.5ms
DT9147 **(* Note 1)**	**DT90147** **(* Note 1)**		The maximum interval between two sending operations: value in the register × 2.5ms

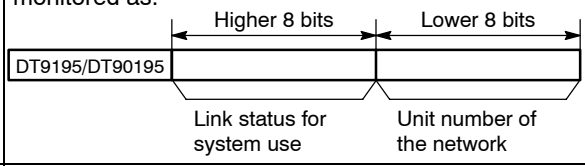
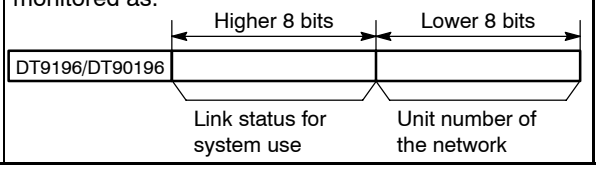
☞ Notes

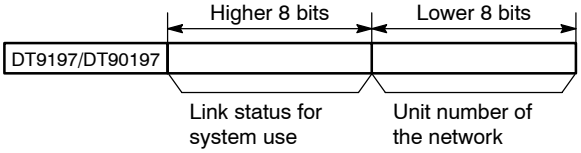
- **(*1): Used by the system.**
- **(*2): When system register 46 = K0, First: PC link 0, second: PC link 1**
  When system register 46 = K1, First: PC link 1, second: PC link 0

Address		Name	Description
FP3	FP10SH		
DT9148 (* Note 1)	DT90148 (* Note 1)	MEWNET-W/-P PC link status [PC link 1 (W/P)] **(* Note 2)**	The number of times the receiving operation is performed (counted using ring counter).
DT9149 (* Note 1)	DT90149 (* Note 1)		The current interval between two receiving operations: value in the register × 2.5ms
DT9150 (* Note 1)	DT90150 (* Note 1)		The minimum interval between two receiving operations: value in the register × 2.5ms
DT9151 (* Note 1)	DT90151 (* Note 1)		The maximum interval between two receiving operations: value in the register × 2.5ms
DT9152 (* Note 1)	DT90152 (* Note 1)		The number of times the sending operation is performed (counted using ring counter).
DT9153 (* Note 1)	DT90153 (* Note 1)		The current interval between two sending operations: value in the register × 2.5ms
DT9154 (* Note 1)	DT90154 (* Note 1)		The minimum interval between two sending operations: value in the register × 2.5ms
DT9155 (* Note 1)	DT90155 (* Note 1)		The maximum interval between two sending operations: value in the register × 2.5ms
DT9156	DT90156	MEWNET-W/-P PC link status [PC link 0 (W/P)] **(* Note 2)**	Area used for measurement of receiving interval.
DT9157	DT90157		Area used for measurement of sending interval.
DT9158	DT90158	MEWNET-W/-P PC link status [PC link 1 (W/P)] **(* Note 2)**	Area used for measurement of receiving interval.
DT9159	DT90159		Area used for measurement of sending interval.
DT9160	DT90160	Link unit No. [W/P link 1]	Stores the unit No. of link 1
DT9161	DT90161	Error flag [W/P link 1]	Stores the error flag of link 1
DT9162	DT90162	Link unit No. [W/P link 2]	Stores the unit No. of link 2
DT9163	DT90163	Error flag [W/P link 2]	Stores the error flag of link 2
DT9164	DT90164	Link unit No. [W/P link 3]	Stores the unit No. of link 3
DT9165	DT90165	Error flag [W/P link 3]	Stores the error flag of link 3
DT9166	DT90166	———	Not used
DT9167	DT90167	———	Not used
DT9168	DT90168	———	Not used
DT9169	DT90169	———	Not used

☞ **Notes**

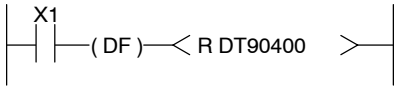
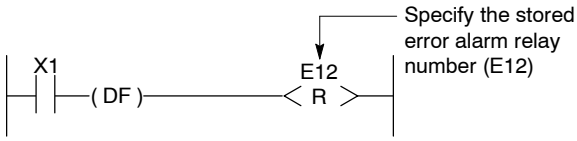
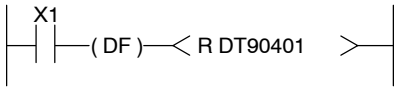
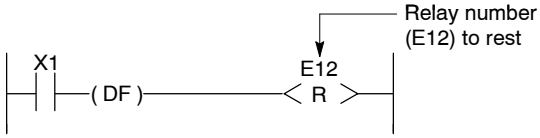
- **(*1): Used by the system.**
- **(*2): When system register 46 = K0, First: PC link 0, second: PC link 1**
  When system register 46 = K1, First: PC link 1, second: PC link 0

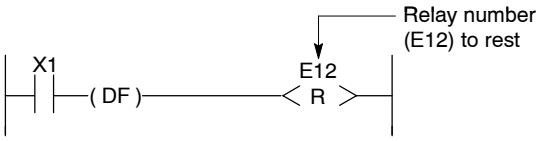
Address		Name	Description
FP3	FP10SH		
DT9170	DT90170	MEWNET-W/-P link status [W/P link 1]	Station number, where the send area address for the PC link is overlapped with this station, is stored here.
DT9171	DT90171		Test result in the optical transmission path test mode for MEWNET−P link system is stored here.
DT9172	DT90172		Counts how many times a token is lost.
DT9173	DT90173		Counts how many times two or more tokens are detected.
DT9174	DT90174		Counts how many times a signal is lost.
DT9175	DT90175		Counts how many times a synchronous abnormality is detected.
DT9176	DT90176		Send NACK
DT9177	DT90177		Send NACK
DT9178	DT90178		Send WACK
DT9179	DT90179		Send WACK
DT9180	DT90180		Send answer
DT9181	DT90181		Send answer
DT9182	DT90182		Unidentified command
DT9183	DT90183		Counts how many times a parity error is detected.
DT9184	DT90184		Counts how many times an end code error is detected.
DT9185	DT90185		Format error
DT9186	DT90186		Not support error
DT9187	DT90187		Self-diagnostic result
DT9188	DT90188		Counts how many times loop change is detected.
DT9189	DT90189		Counts how many times link error is detected.
DT9190	DT90190		Counts how many times main loop break is detected.
DT9191	DT90191		Counts how many times sub loop break is detected.
DT9192	DT90192		Loop reconstructing condition
DT9193	DT90193		Loop operation mode
DT9194	DT90194		Loop input status
DT9195	DT90195	MEWNET−H link status/link unit number in the H link 1 position	The link status for the MEWNET−H link unit is monitored as: 
DT9196	DT90196	MEWNET−H link status/link unit number in the H link 2 position	The link status for the MEWNET−H link unit is monitored as: 

Address		Name	Description
FP3	FP10SH		
DT9197	DT90197	MEWNET−H link status/link unit number in the H link 3 position	The link status for the MEWNET−H link unit is monitored as: 
DT9198	DT90198	———	Not used
DT9199	DT90199	———	Not used
DT9200	DT90200	MEWNET-W/-P link status [W/P link 2]	Station number, where the send area address for the PC link is overlapped with this station, is stored here.
DT9201	DT90201		Test result in the optical transmission path test mode for MEWNET−P link system is stored here.
DT9202	DT90202		Counts how many times a token is lost.
DT9203	DT90203		Counts how many times two or more tokens are detected.
DT9204	DT90204		Counts how many times a signal is lost.
DT9205	DT90205		Counts how many times a synchronous abnormality is detected.
DT9206	DT90206		Send NACK
DT9207	DT90207		Send NACK
DT9208	DT90208		Send WACK
DT9209	DT90209		Send WACK
DT9210	DT90210		Send answer
DT9211	DT90211		Send answer
DT9212	DT90212		Unidentified command
DT9213	DT90213		Counts how many times a parity error is detected.
DT9214	DT90214		Counts how many times an end code error is detected.
DT9215	DT90215		Format error
DT9216	DT90216		Not support error
DT9217	DT90217		Self-diagnostic result
DT9218	DT90218		Counts how many times loop change is detected.
DT9219	DT90219		Counts how many times link error is detected.
DT9220	DT90220		Counts how many times main loop break is detected.
DT9221	DT90221		Counts how many times sub loop break is detected.
DT9222	DT90222		Loop reconstructing condition
DT9223	DT90223		Loop operation mode
DT9224	DT90224		Loop input status
DT9225	DT90225	———	Not used
DT9226	DT90226	———	Not used
DT9227	DT90227	———	Not used
DT9228	DT90228	———	Not used
DT9229	DT90229	———	Not used

Address		Name	Description
FP3	FP10SH		
DT9230	DT90230	MEWNET-W/-P link status [W/P link 3]	Station number, where the send area address for the PC link is overlapped with this station, is stored here.
DT9231	DT90231		Test result in the optical transmission path test mode for MEWNET−P link system is stored here.
DT9232	DT90232		Counts how many times a token is lost.
DT9233	DT90233		Counts how many times two or more tokens are detected.
DT9234	DT90234		Counts how many times a signal is lost.
DT9235	DT90235		Counts how many times a synchronous abnormality is detected.
DT9236	DT90236		Send NACK
DT9237	DT90237		Send NACK
DT9238	DT90238		Send WACK
DT9239	DT90239		Send WACK
DT9240	DT90240		Send answer
DT9241	DT90241		Send answer
DT9242	DT90242		Unidentified command
DT9243	DT90243		Counts how many times a parity error is detected.
DT9244	DT90244		Counts how many times an end code error is detected.
DT9245	DT90245		Format error
DT9246	DT90246		Not support error
DT9247	DT90247		Self-diagnostic result
DT9248	DT90248		Counts how many times loop change is detected.
DT9249	DT90249		Counts how many times link error is detected.
DT9250	DT90250		Counts how many times main loop break is detected.
DT9251	DT90251		Counts how many times sub loop break is detected.
DT9252	DT90252		Loop reconstructing condition
DT9253	DT90253		Loop operation mode
DT9254	DT90254		Loop input status
DT9255 (Not used)	DT90255	Monitoring TOOL port station number (Available PLC: FP10SH)	Station number (range: H1 to H32) set for FP10SH TOOL (RS232C) port is stored here in the BCD expression.
DT9256 (Not used)	DT90256	Monitoring COM port station number (Available PLC: FP10SH)	Station number (range: H1 to H32) set for FP10SH COM (RS232C) port is stored here in the BCD expression.
DT9257 (Not used)	DT90257	Operation error program number (hold) (Available PLC: FP10SH)	An operation error program block number is stored here when an operation error is detected. Program block number − H1: In the first program block − H2: In the 2nd program block

Address		Name	Description
FP3	FP10SH		
DT9258 **(Not used)**	**DT90258**	Operation error program number (non−hold) (Available PLC: FP10SH)	The program block number for the latest operation error is stored here each time an operation error is detected. Program block number − H1: In the first program block − H2: In the 2nd program block
DT9259 **(Not used)**	**DT90259**	Break occurrence program number (Available PLC: FP10SH)	The program block number where the **BRK** instruction occurred is stored here. Program block number − H1: In the first program block − H2: In the 2nd program block
DT9260 **(Not used)**	**DT90260**	Type of IC memory card installed (Available PLC: FP10SH)	Type of IC memory card is monitored here as: − H5: Flash−EEPROM type IC memory card − H6: SRAM type IC memory card − H506: Flash−EEPROM/SRAM mixed type IC memory card − H6: No archival information is stored − H6: No data is written − Other than above: Erroneous condition (* Error code E56)
DT9261 **(Not used)**	**DT90261**	Capacity of IC memory card 1 (Available PLC: FP10SH)	The capacity of IC memory card is stored in units of KB. If Flash−EEPROM/SRAM mixed type IC memory card is used, SRAM capacity is stored.
DT9262 **(Not used)**	**DT90262**	Capacity of IC memory card 2 (Available PLC: FP10SH)	The capacity of IC memory card is stored in units of KB. If Flash−EEPROM/SRAM mixed type IC memory card is used, flash−EEPROM capacity is stored.
DT9263	**DT90263**	———	Not used
DT9264	**DT90264**	———	Not used
DT9265 **(Not used)**	**DT90265**	FP10SH free compile memory capacity (Available PLC: FP10SH)	Free capacity of FP10SH compile memory is stored here. If 120 k steps memory expansion is used, the capacity of the 1st program block number is stored.
DT9266 **(Not used)**	**DT90266**	FP10SH free compile memory capacity for program block 2 (Available PLC: FP10SH)	Free capacity of FP10SH program block 2 compile memory is stored here.
DT9267 **(Not used)**	**DT90267** **(Not used)**	———	Not used
DT9268 **(Not used)**	**DT90268**	Index register bank (current value) (Available PLC: FP10SH)	The current value of index register bank is stored here.
DT9269 **(Not used)**	**DT90269**	Index register bank (shelter number) (Available PLC: FP10SH)	The shelter number of index register bank is stored here.

Address		Name	Description
FP3	FP10SH		
DT9399 (Not used)	**DT90399 (Not used)**	_____	Not used
DT9400 (Not used)	**DT90400**	Number of the error alarm relay which went ON (Available PLC: FP10SH)	The total of the error alarm relay which went ON is stored here. (Max. 500) To reset all data in the error alarm buffer, use an **RST** instruction and DT90400. 
DT9401 (Not used)	**DT90401**	First error alarm relay which went ON (Available PLC: FP10SH)	The first error alarm relay number which went ON is stored. The error has been reset by executing a **RST** instruction. **Example 1: Using RST instruction**  **Example 2: Using RST instruction and DT90401** 
DT9402 (Not used)	**DT90402**	Second error alarm relay which went ON (Available PLC: FP10SH)	The error alarm relay number which went ON is stored. To reset the specified error alarm relay, ues an **RST** instruction. 
DT9403 (Not used)	**DT90403**	Third error alarm relay which went ON (Available PLC: FP10SH)	
DT9404 (Not used)	**DT90404**	Fourth error alarm relay which went ON (Available PLC: FP10SH)	
DT9405 (Not used)	**DT90405**	Fifth error alarm relay which went ON (Available PLC: FP10SH)	
DT9406 (Not used)	**DT90406**	Sixth error alarm relay which went ON (Available PLC: FP10SH)	
DT9407 (Not used)	**DT90407**	Seventh error alarm relay which went ON (Available PLC: FP10SH)	

Address		Name	Description
FP3	FP10SH		
DT9408 **(Not used)**	**DT90408**	Eighth error alarm relay which went ON (Available PLC: FP10SH)	The error alarm relay number which went ON is stored. To reset the specified error alarm relay, ues an **RST** instruction. 
DT9409 **(Not used)**	**DT90409**	Ninth error alarm relay which went ON (Available PLC: FP10SH)	
DT9410 **(Not used)**	**DT90410**	Tenth error alarm relay which went ON (Available PLC: FP10SH)	
DT9411 **(Not used)**	**DT90411**	Eleventh error alarm relay which went ON (Available PLC: FP10SH)	
DT9412 **(Not used)**	**DT90412**	Twelfth error alarm relay which went ON (Available PLC: FP10SH)	
DT9413 **(Not used)**	**DT90413**	Thirteenth error alarm relay which went ON (Available PLC: FP10SH)	
DT9414 **(Not used)**	**DT90414**	Fourteenth error alarm relay which went ON (Available PLC: FP10SH)	
DT9415 **(Not used)**	**DT90415**	Fifteenth error alarm relay which went ON (Available PLC: FP10SH)	
DT9416 **(Not used)**	**DT90416**	Sixteenth error alarm relay which went ON (Available PLC: FP10SH)	
DT9417 **(Not used)**	**DT90417**	Seventeenth error alarm relay which went ON (Available PLC: FP10SH)	
DT9418 **(Not used)**	**DT90418**	Eighteenth error alarm relay which went ON (Available PLC: FP10SH)	
DT9419 **(Not used)**	**DT90419**	Nineteenth error alarm relay which went ON (Available PLC: FP10SH)	

Address		Name	Description
FP3	FP10SH		
DT9420 **(Not used)**	**DT90420**	Time at which the first error alarm relay (DT90401) went ON (for minute and second data) (Available PLC: FP10SH)	The minute and second data at which the first error alarm relay in DT90401 went ON is stored.
DT9421 **(Not used)**	**DT90421**	Time at which the first error alarm relay (DT90401) went ON (for day and hour data) (Available PLC: FP10SH)	The day and hour data at which the first error alarm relay in DT90401 went ON is stored.
DT9422 **(Not used)**	**DT90422**	Time at which the first error alarm relay (DT90401) went ON (for year and month data) (Available PLC: FP10SH)	The year and month data at which the first error alarm relay in DT90401 went ON is stored.

Appendix F

Table of Error Codes

F.1 Confirmation of Error When the Error LED Turns ON

When the “ERROR LED” on the CPU turns ON, a **self-diagnostic error** or **syntax check error** has occurred. Confirm the contents of the error and take the appropriate steps.

F.1.1 Confirmation Method

Procedure:

1. **Use the programming tool to call up the error code.**
   - **Using NPST-GR software:**
     By executing the “STATUS DISPLAY”, the error code and content of error are displayed.
   - **Using FP programmer II Ver.2**
     With the syntax check error, the error code and message is displayed by simply connecting the unit.
     With the self–diagnostic error, press the following keys.
     ACLR (–) OP 1 1 0 ENT READ ▼
     Then the self–diagnostic error code will be displayed.
2. **Check the error contents in the table of error codes of sections F.2 to F.4 using the error code ascertained above.**

F.1.2 Self-Diagnostic Error

This error occurs when the CPU’s self-diagnostic function detects the occurrence of an abnormality in the system. The self-diagnostic function monitors the watching dog timer, memory abnormal detection, I/O abnormal detection, and other devices.

When a self-diagnostic error occurs

- Δ The CPU’s ERROR LED turns ON.
- Δ The operation of the CPU might stop depending on the content of error and the system register setting.
- Δ The error codes will be stored in the special data register DT9000 for FP3 and DT90000 for FP10SH.

☞ next page

Clearing the self-diagnostic error

- **Using NPST-GR software:**
  At the “STATUS DISPLAY”, press the **<F3>** (error clear) key.
  Error codes 43 and higher can be cleared.
- **Using FP programmer II Ver.2:**
  Press the keys as shown below. Error codes 43 and higher can be cleared.
  ACLR (–) OP 1 1 2 ENT SHIFT SC WRT
- You can use the initialize/test switch of CPU to clear an error. However, this will also clear the contents of operation memory.
- Errors can also be cleared by turning OFF and ON the power while in the PROG. mode. However, the contents of operation memory, not stored with the hold type data, will also be cleared.
- The error can also be cleared depending on the self-diagnostic error set instruction **F148 (ERR)**.

Steps to take for self-diagnostic error

The steps to be taken will differ depending on the error contents. For more details, use the error code obtained above and consult the table of self-diagnostic error codes (* section F.3).

F.1.3 Syntax Check Error

This is an error detected by the total check function when there is a syntax error or incorrect setting written in the program. When the mode selector of CPU is switched to the RUN mode, the total check function automatically activates and eliminates the possibility of incorrect operation from syntax errors in the program.

When a syntax check error is detected

ERROR LED turns ON.
Operation will not begin even after switching to the RUN mode.

Clearing a syntax check error

By changing to the PROG. mode, the error will clear and the ERROR LED will turn OFF.

Steps to take for syntax error

Change to the PROG. mode, and then execute the total check function while online mode with the programming tool connected. This will call up the content of error and the address where the error occurred.
Correct the program while referring to the content of error.

F.2 Table of Syntax Check Error

Error code	Name of error	Operation status	Description and steps to take
E1	**Syntax error**	Stops	A program with a syntax error has been written. **Change to PROG. mode and correct the error.**
E2 (* Note)	**Duplicated output error**	Stops	Two or more **OT(Out)** instructions and **KP(Keep)** instructions are programmed using the same relay. **Change to PROG. mode and correct the program so that one relay is not used for two or more OT instructions and KP instructions. Or, set the duplicated output to "enable (K1)" in system register 20. (* sections B.3 and B.4)**
E3	**Not paired error**	Stops	For instructions which must be used in a pair such as jump (**JP** and **LBL**), one instruction is either missing or in an incorrect position. **Change to PROG. mode and enter the two instructions which must be used in a pair in the correct positions.**
E4	**Parameter mismatch error**	Stops	An instruction has been written which does not agree with system register settings. For example, the number setting in a program does not agree with the timer/counter range setting. **Change to PROG. mode, check the system register settings, and change so that the settings and the instruction agree.**
E5 (* Note)	**Program area error**	Stops	An instruction which must be written to a specific area (main program area or subprogram area) has been written to a different area (for example, a subroutine **SUB** to **RET** is placed before an **ED** instruction). **Change to PROG. mode and enter the instruction into the correct area.**
E6	**Compile memory full error (Available PLC: FP10SH)**	Stops	The program stored in the FP10SH is too large to compile in the program memory. **Change to PROG. mode and reduce the total number of steps for the program.**

☞ **Note**

This error is also detected if you attempt to execute a rewrite containing a syntax error during RUN. In this case, nothing will be written to the CPU and operation will continue.

Error code	Name of error	Operation status	Description and steps to take
E7	**High-level instruction type error**	Stops	In the program, high-level instructions, which execute in every scan and at the leading edge of the trigger, are programmed to be triggered by one contact [e.g., **F0 (MV)** and **P0 (PMV)** are programmed using the same trigger continuously]. **Correct the program so that the high-level instructions executed in every scan and only at the leading edge are triggered separately.**
E8	**High-level instruction operand error**	Stops	There is an incorrect operand in an instruction which requires a specific combination operands (for example, the operands must all be of a certain type). **Enter the correct combination of operands.**
E9	**No program error (Available PLC: FP10SH)**	Stops	Program may be damaged. **Try to send the program again using NPST-GR.**
E10	**Rewrite during RUN syntax error**	Continues	When inputting with the ladder symbol mode of NPST-GR, a deletion, addition or change of order of an instruction (**ED**, **LBL**, **SUB**, **RET**, **INT**, **IRET**, **SSTP**, and **STPE**) that cannot perform a rewrite during RUN is being attempted. Nothing is written to the CPU.

F.3 Table of Self-Diagnostic Error

Error code	Name of error	Operation status	Description and steps to take
E20	**CPU error**	Stops	Probably a hardware abnormality. **Please contact your dealer.**
E21 **E22** **E23** **E24** **E25**	**RAM error**	Stops	Probably an abnormality in the internal RAM. **Please contact your dealer.**
E26	**User's ROM error**	Stops	ROM is not installed. There may be a problem with the installed ROM. – ROM contents are damaged – Program size stored on the ROM is larger than the capacity of the ROM **Check the contents of the ROM**
E27	**Intelligent unit installation error**	Stops	Intelligent units installed exceed the limitations (i.e., 4 or more link units) **Turn OFF the power and re-configure intelligent units referring to the hardware manual.**
E28	**System register error**	Stops	Probably an abnormality in the system register. **Check the system register setting or initialize the system registers.**
E29	**System bus time out error (Available PLC: FP3)**	Stops	**Please contact your dealer.**
E30	**Interrupt error 0**	Stops	Probably a hardware abnormality. **Please contact your dealer.**
E31	**Interrupt error 1**	Stops	An interrupt occurred without an interrupt request. A hardware problem or error due to noise is possible. **Turn OFF the power and check the noise conditions.**
E32	**Interrupt error 2**	Stops	An interrupt occurred without an interrupt request. A hardware problem or error due to noise is possible. **Turn OFF the power and check the noise conditions.**
			There is no interrupt program for an interrupt which occurred. **Check the number of the interrupt program and change it to agree with the interrupt request.**

Error code	Name of error	Operation status	Description and steps to take
E33	**Multi-CPU data unmatch error (CPU2 only)**	CPU2 stops	Occurs when a FP3 or FP10SH is used as CPU2 for a multi-CPU system. **Please contact your dealer.**
E34	**I/O status error**	Stops	An abnormal unit is installed. **Check the contents of special data register (FP3: DT9036, FP10SH: DT90036) and locate the abnormal unit.** **Then turn OFF the power and replace the unit with a new one.**
E35	**MEWNET-F (remote I/O) slave illegal unit error**	Stops	A unit, which cannot be installed on the slave station of the MEWNET-F link system, is installed on the slave station. **Remove the illegal unit from the slave station.**
E36	**MEWNET-F limitation error**	Stops	The number of slots or I/O points used for MEWNET-F exceeds the limitation. **Re-configure the system so that the number of slots and I/O points is within the specified range.**
E37	**MEWNET-F I/O mapping error**	Stops	I/O overlap or I/O setting that is over the range is detected in the allocated I/O and MEWNET-F I/O map. **Re-configure the I/O map correctly.**
E38	**MEWNET-F slave I/O mapping error**	Stops	I/O mapping for MEWNET-F I/O terminal boards, remote I/O terminal units and I/O link unit is not correct. **Re-configure the I/O map for slave stations according to the I/O points of the slave stations.**
E39	**IC memory card read error (Available PLC: FP10SH)**	Stops	When reading in the program from the IC memory card (due to automatic reading because of the dip switch 3 setting or program switching due to **F14 (PGRD)** instruction): – IC memory card is not installed. – There is no program file or it is damaged. – Writing is disabled. – There is an abnormality in the AUTOEXEC.SPG file. – Program size stored on the card is larger than the capacity of the unit. **Install a IC memory card that has the program properly recorded and execute the read once again.**

Error code	Name of error	Operation status	Description and steps to take
E40	**MEWNET-TR communica–tion error**	Selectable (using system register 21)	Erroneous MEWNET-TR master unit is detected. **Check the contents of special data registers (FP3: DT9002 and DT9003, FP10SH: DT90002 and DT90003) and locate the output unit with blown fuse or the erroneous MEWNET-TR master unit. Then replace the fuse or check the unit.** **Selection of operation status using system register 21:** **– to continue execution, set K1 (CONT)** **– to stop execution, set K0 (STOP)**
E41	**Intelligent unit error**	Selectable (using system register 22)	An abnormality in an intelligent unit. **Check the contents of special data registers (FP3: DT9006 and DT9007, FP10SH: DT90006 and DT90007) and locate the abnormal intelligent unit. Then check the unit referring to its manual.** **Selection of operation status using system register 22:** **– to continue execution, set K1 (CONT)** **– to stop execution, set K0 (STOP)**
E42	**I/O unit verify error**	Selectable (using system register 23)	I/O unit wiring condition has changed compared to that at time of power-up. **Check the contents of special data registers (FP3: DT9010 and DT9011, FP10SH: DT90010 and DT90011) and locate the erroneous unit. Then check the unit and correct the wiring.** **Selection of operation status using system register 23:** **– to continue execution, set K1 (CONT)** **– to stop execution, set K0 (STOP)**
E43	**System watching dog timer error (Available PLC: FP10SH)**	Selectable (using system register 24)	Scan time required for program execution exceeds the setting of the system watching dog timer. **Check the program and modify it so that FP10SH can execute a scan within the specified time.** **Selection of operation status using system register 24:** **– to continue execution, set K1 (CONT)** **– to stop execution, set K0 (STOP)**

Error code	Name of error	Operation status	Description and steps to take
E45	**Operation error**	Selectable (using system register 26)	Operation became impossible when a high-level instruction was executed. **Check the contents of special data registers (FP3: DT9017 and DT9018, FP10SH: DT90017 and DT90018) to find the program address where the operation error occurred. Then correct the program referring to the description of the instruction.** **Refer to the programming manual.** **Selection of operation status using system register 26:** **– to continue execution, set K1 (CONT)** **– to stop execution, set K0 (STOP)**
E46	**MEWNET-F communica-tion error**	Selectable (using system register 27)	A communication abnormally was caused by a transmission cable or during the power-down of a slave station. **Check the contents of special data registers (FP3: DT9131 to DT9137, FP10SH: DT90131 to DT90137) and locate the abnormal slave station.** **The recover the slave condition referring to the MEWNET-F (REMOTE I/O) SYSTEM manual.** **Selection of operation status using system register 27:** **– to continue execution, set K1 (CONT)** **– to stop execution, set K0 (STOP)**
E47	**MEWNET-F attribute error**	Selectable (using system register 28)	In the unit on the slave station, an abnormality such as: – missing unit – abnormal intelligent unit was detected. **Check the contents of special data registers (FP3: DT9131 to DT9137, FP10SH: DT90131 to DT90137) and locate the abnormal slave station.** **The recover the slave condition referring to the MEWNET-F (REMOTE I/O) SYSTEM manual.** **Selection of operation status using system register 28:** **– to continue execution, set K1 (CONT)** **– to stop execution, set K0 (STOP)**

Error code	Name of error	Operation status	Description and steps to take
E50	**Backup battery error (The BATT. LED turns ON.)**	Continues	The voltage of the backup battery lowered or the backup battery of CPU is not installed. **Check the installation of the backup battery and then replace battery if necessary.** **By setting the system register 4 in K0 (NO), you can disregard this error. However, the BATT. LED turns ON.**
E51	**MEWNET-F terminal station error**	Continues	Terminal station settings were not properly performed. **Check stations at both ends of the communication path, and set them in the terminal station using the dip switches.**
E52	**MEWNET-F I/O update synchronous error**	Continues	**Set the INITIALIZE/TEST selector to the INITIALIZE position while keeping the mode selector in the RUN position. If the same error occurs after this, please contact your dealer.**
E53	**Multi-CPU registration error (CPU2 only)**	Continues	Abnormality was detected when the multi-CPU system was used. **Please contact your dealer.**
E54	**IC memory card backup battery error (The BATT. LED does not turn ON) (Available PLC: FP10SH)**	Continues	The contents of the IC memory card cannot be guaranteed since the voltage of the backup battery for the FP10SH IC memory card lowered. **Replace the backup battery of the FP10SH IC memory card.** **By setting the system register 4 in K0 (NO), you can disregard this error.**
E55	**IC memory card backup battery error (The BATT. LED does not turn ON) (Available PLC: FP10SH)**	Continues	The voltage of the backup battery for FP10SH IC memory card lowers. **Replace the backup battery of the FP10SH IC memory card.** **By setting the system register 4 in K0 (NO), you can disregard this error.**
E56	**Incompatible IC memory card error (Available PLC: FP10SH)**	Continues	The IC memory card installed is not compatible with FP10SH. **Replace the IC memory card compatible with FP10SH.**
E68	**Rewrite during RUN error**	Continues	When inputting with the boolean ladder mode, editing of an instruction (**ED**, **SUB**, **RET**, **INT**, **IRET**, **SSTP**, and **STPE**) that cannot perform a rewrite during RUN is being attempted. Nothing is written to the CPU.

F.3 Table of Self-Diagnostic Error

Error code	Name of error	Operation status	Description and steps to take
E100 to E199	**Self-diagnostic error set by F148 (ERR)/ P148 (PERR) instruction**	Stops	The self-diagnostic error specified by the **F148 (ERR)/P148 (PERR)** instruction is occurred. **Take steps to clear the error condition according to the specification you chose.**
E200 to E299		Continues	

F.4 Table of Communication Check Error

Error code	Name of error	Operation status	Description and steps to take
E63	**Programmable controller error mode**	Stops	Transfer was attempted in the RUN mode. **Switch the mode and execute once again.**
E64	**No ROM/RAM error**	Stops	An abnormality occurred when loading RAM to ROM. There may be a problem with the ROM or IC memory card. – When loading, the specified contents exceeded the capacity (256 KB). – Write error occurs. – ROM or IC memory card is not installed. – ROM or IC memory card does not conform to specifications. **Check the contents of the ROM or IC memory card.**
E65	**Protect error**	Stops	Transfer was attempted during ROM operation or when the protect switch was ON. **Switch the mode and execute once again.**

F.4 Table of Communication Check Error

Appendix G

Table of Instructions

G.1 Table of Basic Instructions

Name	Boolean	Symbol	Description	Steps	Availability	
					FP3	FP10SH
Basic sequence instructions						
Start	**ST**	X,Y,R,T,C,L,P,E	Begins a logic operation with a Form A (normally open) contact.	**1 (2)** **(* Note 1)**	**A**	**A**
Start not	**ST/**	X,Y,R,T,C,L,P,E	Begins a logic operation with a Form B (normally closed) contact.	**1 (2)** **(* Note 1)**	**A**	**A**
Out	**OT**	Y,R,L,E	Outputs the operated result to the specified output.	**1 (2)** **(* Note 1)**	**A**	**A**
Not	**/**		Inverts the operated result up to this instruction.	**1**	**A**	**A**
AND	**AN**	X,Y,R,T,C,L,P,E	Connects a Form A (normally open) contact serially.	**1 (2)** **(* Note 1)**	**A**	**A**
AND not	**AN/**	X,Y,R,T,C,L,P,E	Connects a Form B (normally closed) contact serially.	**1(2)** **(* Note 1)**	**A**	**A**
OR	**OR**	X,Y,R,T,C,L,P,E	Connects a Form A (normally open) contact in parallel.	**1 (2)** **(* Note 1)**	**A**	**A**
OR not	**OR/**	X,Y,R,T,C,L,P,E	Connects a Form B (normally closed) contact in parallel.	**1 (2)** **(* Note 1)**	**A**	**A**
Leading edge start	**ST↑**	X,Y,R,T,C,L,P,E	Begins a logic operation only for one scan when the leading edge of the trigger is detected.	**2**	**N/A**	**A** **(* Note 2)**
Trailing edge start	**ST↓**	X,Y,R,T,C,L,P,E	Begins a logic operation only for one scan when the trailing edge of the trigger is detected.	**2**	**N/A**	**A** **(* Note 2)**

☞ **Notes**

- **A: Available, N/A: Not available**
- **(*1): In the FP10SH, when using X1280, Y1280, R1120, L1280, T256, C256 or anything beyond for the ST, ST/, OT, AN, AN/, OR and OR/ instructions, the number of steps is shown in parentheses. Also, in the FP10SH, when a relay number has an index modifier, the number of steps is shown in parentheses.**

- **(*2): This instruction should be input using NPST−GR Ver.4.0 or later.**

Name	Boolean	Symbol	Description	Steps	Availability	
					FP3	FP10SH
Leading edge AND	**AN↑**	X,Y,R,T,C,L,P,E	Connects a Form A (normally open) contact serially only for one scan when the leading edge of the trigger is detected.	**2**	**N/A**	**A (* Note 1)**
Trailing edge AND	**AN↓**	X,Y,R,T,C,L,P,E	Connects a Form A (normally open) contact serially only for one scan when the trailing edge of the trigger is detected.	**2**	**N/A**	**A (* Note 1)**
Leading edge OR	**OR↑**	X,Y,R,T,C,L,P,E	Connects a Form A (normally open) contact in parallel only for one scan when the leading edge of the trigger is detected.	**2**	**N/A**	**A (* Note 1)**
Trailing edge OR	**OR↓**	X,Y,R,T,C,L,P,E	Connects a Form A (normally open) contact in parallel only for one scan when the trailing edge of the trigger is detected.	**2**	**N/A**	**A (* Note 1)**
Leading edge out	**OT↑**	P	Outputs the operated result to the specified output only for one scan when leading edge of the trigger is detected. (for pulse relay)	**2**	**N/A**	**A (* Note 1)**
Trailing edge out	**OT↓**	P	Outputs the operated result to the specified output only for one scan when trailing edge of the trigger is detected. (for pulse relay)	**2**	**N/A**	**A (* Note 1)**
Alternative out	**ALT**	Y,R,L,E A	Inverts the output condition (ON/OFF) each time the leading edge of the trigger is detected.	**3**	**N/A**	**A (* Note 1)**
AND stack	**ANS**		Connects the multiple instruction blocks serially.	**1**	**A**	**A**
OR stack	**ORS**		Connects the multiple instruction blocks in parallel.	**1**	**A**	**A**

☞ **Notes**

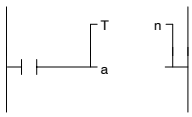
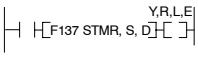
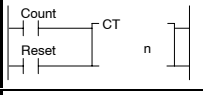
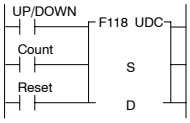
- **A: Available, N/A: Not available**
- **(*1): This instruction should be input using NPST−GR Ver.4.0 or later.**

G.1 Table of Basic Instructions

Name	Boolean	Symbol	Description	Steps	Availability	
					FP3	FP10SH
Push stack	**PSHS**		Stores the operated result up to this instruction.	**1**	**A**	**A**
Read stack	**RDS**		Reads the operated result stored by the **PSHS** instruction.	**1**	**A**	**A**
Pop stack	**POPS**		Reads and clears the operated result stored by the **PSHS** instruction.	**1**	**A**	**A**
Leading edge differential	**DF**	(DF)	Turns ON the contact for only one scan when the leading edge of the trigger is detected.	**1**	**A**	**A**
Trailing edge differential	**DF/**	(DF/)	Turns ON the contact for only one scan when the trailing edge of the trigger is detected.	**1**	**A**	**A**
Leading edge differential (initial execution type)	**DFI**	(DFI)	Turns ON the contact for only one scan when the leading edge of the trigger is detected. The leading edge detection is possible on the first scan.	**1**	**N/A**	**A** **(* Note 1)**
Set	**SET**	Y,R,L,E < S >	Output is set to and held at ON.	**3**	**A** **(* Note 2)**	**A**
Reset	**RST**	Y,R,L,E < R >	Output is set to and held at OFF.	**3**	**A** **(* Note 2)**	**A**
Keep	**KP**	Set Reset KP	Outputs at set trigger and holds until reset trigger turns ON.	**1**	**A**	**A**
No operation	**NOP**	— • —	No operation.	**1**	**A**	**A**

☞ **Notes**

- **A: Available, N/A: Not available**
- **(*1): This instruction should be input using NPST–GR Ver.4.0 or later.**
- **(*2): This instruction is available for FP3 CPU Ver.3.1 or later.**

Name	Boolean	Symbol	Description	Steps	Availability	
					FP3	FP10SH
Basic function instructions						
ON-delay timer	**TML**		After set value “n” **(* Note 1)** × 0.001 seconds, timer contact “a” is set to ON.	**3 (4)** **(* Note 2)**	**N/A**	**A** **(* Note 3)**
	TMR		After set value “n” **(* Note 1)** × 0.01 seconds, timer contact “a” is set to ON.	**3 (4)** **(* Note 2)**	**A**	**A**
	TMX		After set value “n” **(* Note 1)** × 0.1 seconds, timer contact “a” is set to ON.	**3 (4)** **(* Note 2)**	**A**	**A**
	TMY		After set value “n” **(* Note 1)** × 1 second, timer contact “a” is set to ON.	**4 (5)** **(* Note 2)**	**A**	**A**
Auxiliary timer	**F137 (STMR)**		After set value “S” × 0.01 seconds, the specified output **(* Note 4)** and R900D are set to ON.	**5**	**A** **(* Note 5)**	**A**
Counter	**CT**		Decrements from the preset value “n” **(* Note 1)**.	**4 (3)** **(* Note 2)**	**A**	**A**
UP/DOWN counter	**F118 (UDC)**		Increments or decrements from the preset value “S” based on up/down input.	**5**	**A**	**A**

☞ Notes

- **A: Available, N/A: Not available**
- **(*1): The set value “n” can be specified by the set value area number using FP3/FP10SH CPU Ver.4.4 or later.**
  The set value “n” should be input using NPST–GR Ver.3.1 or later and FP programmer II (AFP1114V2).
- **(*2): When timer 256 or higher, or counter 255 or lower, is used, the number of steps is the number in parentheses. Also, when a timer number or counter number has an index modifier, the number of steps is the number in parentheses.**
- **(*3): This instruction should be input using NPST–GR Ver.4.0 or later.**
- **(*4): An OT instruction can be input after an auxiliary timer instruction using FP3/FP10SH CPU Ver.4.0 or later.**
  This instruction should be input using NPST–GR Ver.2.3 or later and FP programmer II (AFP1114V2).
- **(*5): This instruction is available for FP3 CPU Ver.3.1 or later.**

G.1 Table of Basic Instructions

Name	Boolean	Symbol	Description	Steps	Availability	
					FP3	FP10SH
Shift register	**SR**	Data, Shift, Reset, SR WR n	Shifts one bit of 16-bit [word internal relay (WR)] data to the left.	**1 (2)** **(* Note 1)**	**A**	**A**
Left/right shift register	**F119 (LRSR)**	L/R, Data, Shift, Reset, F119 LRSR, D1, D2	Shifts one bit of 16-bit data range specified by “D1” and “D2” to the left or to the right.	**5**	**A**	**A**
Control instructions						
Master control relay	**MC**	(MC n) Master control area	Starts the master control program.	**2**	**A**	**A**
Master control relay end	**MCE**	(MCE n)	Ends the master control program.	**2**	**A**	**A**
Jump **Label**	**JP** **LBL**	(JP n) (LBL n)	The program jumps to the label instruction and continues from there.	**2 (3)** **(* Note 2)** **1**	**A**	**A**
Auxiliary jump **Label**	**F19** **LBL**	[F19 SJP S] (LBL n)	The program jumps to the label instruction specified by “S” and continues from there.	**3** **1**	**A**	**A**
Loop **Label**	**LOOP** **LBL**	(LBL n) [LOOP n, S]	The program jumps to the label instruction and continues from there (the number of jumps is set in “S”).	**4 (5)** **(* Note 2)** **1**	**A**	**A**
Break	**BRK**	(BRK)	Stops program execution when the predetermined trigger turns ON in the TEST/RUN mode only.	**1**	**A**	**A**

☞ Notes

- **A: Available**
- **(*1): In the FP10SH, when internal relay WR240 or higher is used, the number of steps is the number in parentheses. Also, in the FP10SH, when the specified internal relay number (word address) has an index modifier, the number of steps is the number in parentheses.**
- **(*2): In the FP10SH, when the number “n” in a jump or loop instruction has an index modifier, the number of steps is the number in parentheses.**

Name	Boolean	Symbol	Description	Steps	Availability	
					FP3	FP10SH
End	**ED**	(ED)	The operation of program is ended. Indicates the end of a main program.	**1**	**A**	**A**
Conditional end	**CNDE**	(CNDE)	The operation of program is ended when the trigger turns ON.	**1**	**A**	**A**
Step ladder instructions						
Start step	**SSTP**	(SSTP n)	The start of program “n” for process control.	**3**	**A**	**A**
Next step	**NSTL**	(NSTL n)	Start the specified process “n” and clear the process currently started. (Scan execution type)	**3**	**A** (* Note 1)	**A**
	NSTP	(NSTP n)	Start the specified process “n” and clear the process currently started. (Pulse execution type)	**3**	**A**	**A**
Clear step	**CSTP**	(CSTP n)	Resets the specified process.	**3**	**A**	**A**
Clear multiple steps	**SCLR**	[SCLR n1, n2]	Resets multiple processes specified by “n1” and “n2.”	**5**	**N/A**	**A** (* Note 2)
Step end	**STPE**	(STPE)	End of step ladder area.	**1**	**A**	**A**
Subroutine instructions						
Subroutine call	**CALL**	(CALL n)	Executes the specified subroutine. When returning to the main program, outputs in the subroutine program are maintained.	**2 (3)** (* Note 3)	**A**	**A** (* Note 2)

☞ Notes

- **A: Available, N/A: Not available**
- **(*1): This instruction is available for FP3 CPU Ver.4.0 or later. It should be input using NPST−GR Ver.2.3 or later and FP programmer II (AFP1114V2).**
- **(*2): This instruction should be input using NPST−GR Ver.4.0 or later.**
- **(*3): When the number “n” of a subroutine program has an index modifier, the number of steps is the number in parentheses.**

G.1 Table of Basic Instructions

Name	Boolean	Symbol	Description	Steps	Availability	
					FP3	FP10SH
Output OFF type subroutine call	**FCAL**	(FCAL n)	Executes the specified subroutine. When returning to the main program, all outputs in the subroutine program are set to OFF.	**4**	**N/A**	**A (* Note 1)**
Subroutine entry	**SUB**	(SUB n)	Indicates the start of the subroutine program.	**1**	**A**	**A**
Subroutine return	**RET**	(RET)	Ends the subroutine program.	**1**	**A**	**A**
Interrupt instructions						
Interrupt	**INT**	(INT n)	Indicates the start of the interrupt program.	**1**	**A**	**A**
Interrupt return	**IRET**	(IRET)	Ends the interrupt program.	**1**	**A**	**A**
Interrupt control	**ICTL**	(DF) ICTL S1, S2	Select interrupt enable/disable or clear in “S1” and “S2” and execute.	**5**	**A**	**A**

☞ Notes

- **A: Available, N/A: Not available**
- **(*1): This instruction should be input using NPST–GR Ver.4.0 or later.**

Name	Boolean	Symbol	Description	Steps	Availability	
					FP3	FP10SH
Data compare instructions						
16-bit data compare (Start)	**ST=**	= S1, S2	Begins a logic operation by comparing two 16-bit data in the comparative condition “S1=S2.”	**5**	**A** (* Note 1)	**A**
	ST<>	< > S1, S2	Begins a logic operation by comparing two 16-bit data in the comparative condition “S1≠S2.”	**5**	**A** (* Note 1)	**A**
	ST>	> S1, S2	Begins a logic operation by comparing two 16-bit data in the comparative condition “S1>S2.”	**5**	**A** (* Note 1)	**A**
	ST>=	> = S1, S2	Begins a logic operation by comparing two 16-bit data in the comparative condition “S1≧S2.”	**5**	**A** (* Note 1)	**A**
	ST<	< S1, S2	Begins a logic operation by comparing two 16-bit data in the comparative condition “S1<S2.”	**5**	**A** (* Note 1)	**A**
	ST<=	< = S1, S2	Begins a logic operation by comparing two 16-bit data in the comparative condition “S1≦S2.”	**5**	**A** (* Note 1)	**A**

☞ Notes

- **A: Available**
- **(*1): This instruction is available for FP3 CPU Ver.4.4 or later. The instruction should be input using NPST−GR Ver.3.1 or later and FP programmer II (AFP1114V2).**

G.1 Table of Basic Instructions

Name	Boolean	Symbol	Description	Steps	Availability	
					FP3	FP10SH
16-bit data compare (AND)	**AN=**	= S1, S2	Connects a Form A (normally open) contact serially by comparing two 16-bit data in the comparative condition “S1=S2.”	**5**	**A** (* Note 1)	**A**
	AN<>	< > S1, S2	Connects a Form A (normally open) contact serially by comparing two 16-bit data in the comparative condition “S1≠S2.”	**5**	**A** (* Note 1)	**A**
	AN>	> S1, S2	Connects a Form A (normally open) contact serially by comparing two 16-bit data in the comparative condition “S1>S2.”	**5**	**A** (* Note 1)	**A**
	AN>=	> = S1, S2	Connects a Form A (normally open) contact serially by comparing two 16-bit data in the comparative condition “S1≧S2.”	**5**	**A** (* Note 1)	**A**
	AN<	< S1, S2	Connects a Form A (normally open) contact serially by comparing two 16-bit data in the comparative condition “S1<S2.”	**5**	**A** (* Note 1)	**A**
	AN<=	< = S1, S2	Connects a Form A (normally open) contact serially by comparing two 16-bit data in the comparative condition “S1≦S2.”	**5**	**A** (* Note 1)	**A**

☞ **Notes**

- **A: Available**
- **(*1): This instruction is available for FP3 CPU Ver.4.4 or later. The instruction should be input using NPST−GR Ver.3.1 or later and FP programmer II (AFP1114V2).**

Name	Boolean	Symbol	Description	Steps	Availability	
					FP3	FP10SH
16-bit data compare (OR)	**OR=**	= S1, S2	Connects a Form A (normally open) contact in parallel by comparing two 16-bit data in the comparative condition “S1=S2.”	**5**	**A** (* Note 1)	**A**
	OR<>	< > S1, S2	Connects a Form A (normally open) contact in parallel by comparing two 16-bit data in the comparative condition “S1 ≠ S2.”	**5**	**A** (* Note 1)	**A**
	OR>	> S1, S2	Connects a Form A (normally open) contact in parallel by comparing two 16-bit data in the comparative condition “S1>S2.”	**5**	**A** (* Note 1)	**A**
	OR>=	> = S1, S2	Connects a Form A (normally open) contact in parallel by comparing two 16-bit data in the comparative condition “S1 ≧ S2.”	**5**	**A** (* Note 1)	**A**
	OR<	< S1, S2	Connects a Form A (normally open) contact in parallel by comparing two 16-bit data in the comparative condition “S1<S2.”	**5**	**A** (* Note 1)	**A**
	OR<=	< = S1, S2	Connects a Form A (normally open) contact in parallel by comparing two 16-bit data in the comparative condition “S1 ≦ S2.”	**5**	**A** (* Note 1)	**A**

☞ Notes

- **A: Available**
- **(*1): This instruction is available for FP3 CPU Ver.4.4 or later. The instruction should be input using NPST–GR Ver.3.1 or later and FP programmer II (AFP1114V2).**

Name	Boolean	Symbol	Description	Steps	Availability	
					FP3	FP10SH
32-bit data compare (Start)	**STD=**	D= S1, S2	Begins a logic operation by comparing two 32-bit data in the comparative condition “(S1+1, S1)= (S2+1, S2).”	**9**	**A** (* Note 1)	**A**
	STD<>	D< > S1, S2	Begins a logic operation by comparing two 32-bit data in the comparative condition “(S1+1, S1) ≠ (S2+1, S2).”	**9**	**A** (* Note 1)	**A**
	STD>	D> S1, S2	Begins a logic operation by comparing two 32-bit data in the comparative condition “(S1+1, S1)> (S2+1, S2).”	**9**	**A** (* Note 1)	**A**
	STD>=	D> = S1, S2	Begins a logic operation by comparing two 32-bit data in the comparative condition “(S1+1, S1) ≧ (S2+1, S2).”	**9**	**A** (* Note 1)	**A**
	STD<	D< S1, S2	Begins a logic operation by comparing two 32-bit data in the comparative condition “(S1+1, S1)< (S2+1, S2).”	**9**	**A** (* Note 1)	**A**
	STD<=	D< = S1, S2	Begins a logic operation by comparing two 32-bit data in the comparative condition “(S1+1, S1) ≦ (S2+1, S2).”	**9**	**A** (* Note 1)	**A**

☞ Notes

- **A: Available**
- **(*1): This instruction is available for FP3 CPU Ver.4.4 or later. The instruction should be input using NPST−GR Ver.3.1 or later and FP programmer II (AFP1114V2).**

Name	Boolean	Symbol	Description	Steps	Availability	
					FP3	FP10SH
32-bit data compare (AND)	**AND=**	D= S1, S2	Connects a Form A (normally open) contact serially by comparing two 32-bit data in the comparative condition "(S1+1, S1)=(S2+1, S2)."	**9**	**A** (* Note 1)	**A**
	AND<>	D< > S1, S2	Connects a Form A (normally open) contact serially by comparing two 32-bit data in the comparative condition "(S1+1, S1) ≠ (S2+1, S2)."	**9**	**A** (* Note 1)	**A**
	AND>	D> S1, S2	Connects a Form A (normally open) contact serially by comparing two 32-bit data in the comparative condition "(S1+1, S1)>(S2+1, S2)."	**9**	**A** (* Note 1)	**A**
	AND>=	D> = S1, S2	Connects a Form A (normally open) contact serially by comparing two 32-bit data in the comparative condition "(S1+1, S1) ≧ (S2+1, S2)."	**9**	**A** (* Note 1)	**A**
	AND<	D< S1, S2	Connects a Form A (normally open) contact serially by comparing two 32-bit data in the comparative condition "(S1+1, S1)<(S2+1, S2)."	**9**	**A** (* Note 1)	**A**
	AND<=	D< = S1, S2	Connects a Form A (normally open) contact serially by comparing two 32-bit data in the comparative condition "(S1+1, S1) ≦ (S2+1, S2)."	**9**	**A** (* Note 1)	**A**

☞ Notes

- **A: Available**
- **(*1): This instruction is available for FP3 CPU Ver.4.4 or later. The instruction should be input using NPST–GR Ver.3.1 or later and FP programmer II (AFP1114V2).**

Name	Boolean	Symbol	Description	Steps	Availability	
					FP3	FP10SH
32-bit data compare (OR)	**ORD=**	D= S1, S2	Connects a Form A (normally open) contact in parallel by comparing two 32-bit data in the comparative condition “(S1+1, S1)=(S2+1, S2).”	**9**	**A** (* Note 1)	**A**
	ORD<>	D< > S1, S2	Connects a Form A (normally open) contact in parallel by comparing two 32-bit data in the comparative condition “(S1+1, S1) ≠ (S2+1, S2).”	**9**	**A** (* Note 1)	**A**
	ORD>	D> S1, S2	Connects a Form A (normally open) contact in parallel by comparing two 32-bit data in the comparative condition “(S1+1, S1)>(S2+1, S2).”	**9**	**A** (* Note 1)	**A**
	ORD>=	D> = S1, S2	Connects a Form A (normally open) contact in parallel by comparing two 32-bit data in the comparative condition “(S1+1, S1) ≧ (S2+1, S2).”	**9**	**A** (* Note 1)	**A**
	ORD<	D< S1, S2	Connects a Form A (normally open) contact in parallel by comparing two 32-bit data in the comparative condition “(S1+1, S1)<(S2+1, S2).”	**9**	**A** (* Note 1)	**A**
	ORD<=	D< = S1, S2	Connects a Form A (normally open) contact in parallel by comparing two 32-bit data in the comparative condition “(S1+1, S1) ≦ (S2+1, S2).”	**9**	**A** (* Note 1)	**A**

☞ Notes

- **A: Available**
- **(*1): This instruction is available for FP3 CPU Ver.4.4 or later. The instruction should be input using NPST−GR Ver.3.1 or later and FP programmer II (AFP1114V2).**

G.2 Table of High-Level Instructions

The high-level instructions for FP3/FP10SH are expressed by the prefixes “F” or “P” with numbers. For most of the high-level instructions, “F” and “P” types are available. The differences between the two types are explained as follows:

– Instructions with the prefix “F” are executed in every scan while its trigger is in the ON.

– Instructions with the prefix “P” are executed only when the leading edge of its trigger is detected.

Number	Name	Boolean	Operand	Description	Steps	Availability	
						FP3	FP10SH
Data transfer instructions							
F0 P0	**16-bit data move**	**MV PMV**	S, D	(S) → (D)	**5**	**A**	**A**
F1 P1	**32-bit data move**	**DMV PDMV**	S, D	(S+1, S) → (D+1, D)	**7**	**A**	**A**
F2 P2	**16-bit data invert and move**	**MV/ PMV/**	S, D	($\overline{S}$) → (D)	**5**	**A**	**A**
F3 P3	**32-bit data invert and move**	**DMV/ PDMV/**	S, D	($\overline{S+1, S}$) → (D+1, D)	**7**	**A**	**A**
F5 P5	**Bit data move**	**BTM PBTM**	S, n, D	The specified one bit in “S” is transferred to the specified one bit in “D.” The bit is specified by “n.”	**7**	**A**	**A**
F6 P6	**Hexadecimal digit (4-bit) data move**	**DGT PDGT**	S, n, D	The specified one digit in “S” is transferred to the specified one digit in “D.” The digit is specified by “n.”	**7**	**A**	**A**
F7 P7	**Two 16-bit data move**	**MV2 PMV2**	S1, S2, D	(S1) → (D), (S2) → (D+1)	**7**	**N/A**	**A (* Note 1)**
F8 P8	**Two 32-bit data move**	**DMV2 PDMV2**	S1, S2, D	(S1+1, S1) → (D+1, D), (S2+1, S2) → (D+3, D+2)	**11**	**N/A**	**A (* Note 1)**
F10 P10	**Block move**	**BKMV PBKMV**	S1, S2, D	The data between “S1” and “S2” is transferred to the area starting at “D.”	**7**	**A**	**A**

☞ **Notes**

- **A: Available, N/A: Not available**

- **(*1): The instruction for FP10SH should be input using NPST−GR Ver.4.0 or later.**

Number	Name	Boolean	Operand	Description	Steps	Availability	
						FP3	FP10SH
F11 P11	**Block copy**	**COPY PCOPY**	S, D1, D2	The data of “S” is transferred to the all area between “D1” and “D2.”	**7**	**A**	**A**
F12 P12	**Data read from IC memory card**	**ICRD PICRD**	S1, S2, D	The data stored in the expansion memory of the IC memory card specified by “S1” and “S2” are transferred to the area starting at “D.”	**11**	**N/A**	**A**
F13 P13	**Data write to IC memory card**	**ICWT PICWT**	S1, S2, D	The data specified by “S1” and “S2” are transferred to the IC memory card expansion memory area starting at “D.”	**11**	**N/A**	**A**
F14 P14	**Program read from IC memory card**	**PGRD PPGRD**	S	The program specified using “S” is transferred into the FP10SH CPU from IC memory card and executes it.	**3**	**N/A**	**A**
F15 P15	**16-bit data exchange**	**XCH PXCH**	D1, D2	(D1) → (D2), (D2) → (D1)	**5**	**A**	**A**
F16 P16	**32-bit data exchange**	**DXCH PDXCH**	D1, D2	(D1+1, D1) → (D2+1, D2) (D2+1, D2) → (D1+1, D1)	**5**	**A**	**A**
F17 P17	**Higher/lower byte in 16-bit data exchange**	**SWAP PSWAP**	D	The higher byte and lower byte of “D” are exchanged.	**3**	**A**	**A**
F18 P18	**16-bit data block exchange**	**BXCH PBXCH**	D1, D2, D3	Exchange the data between “D1” and “D2” with the data specified by “D3.”	**7**	**N/A**	**A (* Note 1)**
Control instruction							
F19	**Auxiliary jump**	**SJP**	S	The program jumps to the label instruction specified by “S” and continues from there.	**3**	**A**	**A**

☞ **Notes**

- **A: Available, N/A: Not available**
- **(*1): The instruction for FP10SH should be input using NPST–GR Ver.4.0 or later.**

Number	Name	Boolean	Operand	Description	Steps	Availability	
						FP3	FP10SH
Binary arithmetic instructions							
F20 P20	**16-bit data addition**	**+ P+**	S, D	(D) + (S) → (D)	**5**	**A**	**A**
F21 P21	**32-bit data addition**	**D+ PD+**	S, D	(D +1, D) + (S+1, S) → (D+1, D)	**7**	**A**	**A**
F22 P22	**16-bit data addition**	**+ P+**	S1, S2, D	(S1) + (S2) → (D)	**7**	**A**	**A**
F23 P23	**32-bit data addition**	**D+ PD+**	S1, S2, D	(S1+1, S1) + (S2+1, S2) → (D+1, D)	**11**	**A**	**A**
F25 P25	**16-bit data subtraction**	**– P–**	S, D	(D) – (S) → (D)	**5**	**A**	**A**
F26 P26	**32-bit data subtraction**	**D– PD–**	S, D	(D+1, D) – (S+1, S) → (D+1, D)	**7**	**A**	**A**
F27 P27	**16-bit data subtraction**	**– P–**	S1, S2, D	(S1) – (S2) → (D)	**7**	**A**	**A**
F28 P28	**32-bit data subtraction**	**D– PD–**	S1, S2, D	(S1+1, S1) – (S2+1, S2) → (D+1, D)	**11**	**A**	**A**
F30 P30	**16-bit data multiplication**	*** P***	S1, S2, D	(S1) × (S2) → (D+1, D)	**7**	**A**	**A**
F31 P31	**32-bit data multiplication**	**D* PD***	S1, S2, D	(S1+1, S1) × (S2+1, S2) → (D+3, D+2, D+1, D)	**11**	**A**	**A**
F32 P32	**16-bit data division**	**% P%**	S1, S2, D	(S1) ÷ (S2) → quotient (D) remainder (DT9015 for FP3 or DT90015 for FP10SH)	**7**	**A**	**A**
F33 P33	**32-bit data division**	**D% PD%**	S1, S2, D	[(S1+1, S1) ÷ (S2+1, S2) → quotient (D+1, D) remainder (DT9016, DT9015 for FP3 or DT90016, DT90015 for FP10SH)]	**11**	**A**	**A**
F34 P34	**16-bit data multiplication (result in 16 bits)**	***W P*W**	S1, S2, D	(S1) × (S2) → (D)	**7**	**N/A**	**A (* Note 1)**
F35 P35	**16-bit data increment**	**+1 P+1**	D	(D) + 1 → (D)	**3**	**A**	**A**

☞ Notes

- **A: Available, N/A: Not available**
- **(*1): The instruction for FP10SH should be input using NPST–GR Ver.4.0 or later.**

Number	Name	Boolean	Operand	Description	Steps	Availability	
						FP3	FP10SH
F36 P36	**32-bit data increment**	**D+1 PD+1**	D	(D+1, D) + 1 → (D+1, D)	**3**	**A**	**A**
F37 P37	**16-bit data decrement**	**–1 P–1**	D	(D) – 1 → (D)	**3**	**A**	**A**
F38 P38	**32-bit data decrement**	**D–1 PD–1**	D	(D+1, D) – 1 → (D+1, D)	**3**	**A**	**A**
F39 P39	**32-bit data multiplication (result in 32 bits)**	**D*D PD*D**	S1, S2, D	(S1+1, S1) × (S2+1, S2) → (D+1, D)	**11**	**N/A**	**A (* Note 1)**
BCD arithmetic instructions							
F40 P40	**4-digit BCD data addition**	**B+ PB+**	S, D	(D) + (S) → (D)	**5**	**A**	**A**
F41 P41	**8-digit BCD data addition**	**DB+ PDB+**	S, D	(D+1, D) + (S+1, S) → (D+1, D)	**7**	**A**	**A**
F42 P42	**4-digit BCD data addition**	**B+ PB+**	S1, S2, D	(S1) + (S2) → (D)	**7**	**A**	**A**
F43 P43	**8-digit BCD data addition**	**DB+ PDB+**	S1, S2, D	(S1+1, S1) + (S2+1, S2) → (D+1, D)	**11**	**A**	**A**
F45 P45	**4-digit BCD data subtraction**	**B– PB–**	S, D	(D) – (S) → (D)	**5**	**A**	**A**
F46 P46	**8-digit BCD data subtraction**	**DB– PDB–**	S, D	(D+1, D) – (S+1, S) → (D+1, D)	**7**	**A**	**A**
F47 P47	**4-digit BCD data subtraction**	**B– PB–**	S1, S2, D	(S1) – (S2) → (D)	**7**	**A**	**A**
F48 P48	**8-digit BCD data subtraction**	**DB– PDB–**	S1, S2, D	(S1+1, S1) – (S2+1, S2) → (D+1, D)	**11**	**A**	**A**
F50 P50	**4-digit BCD data multiplication**	**B* PB***	S1, S2, D	(S1) × (S2) → (D+1, D)	**7**	**A**	**A**
F51 P51	**8-digit BCD data multiplication**	**DB* PDB***	S1, S2, D	(S1+1, S1) × (S2+1, S2) → (D+3, D+2, D+1, D)	**11**	**A**	**A**

☞ Notes

- **A: Available, N/A: Not available**
- **(*1): The instruction for FP10SH should be input using NPST–GR Ver.4.0 or later.**

G.2 Table of High-Level Instructions

Number	Name	Boolean	Operand	Description	Steps	Availability	
						FP3	FP10SH
F52 P52	**4-digit BCD data division**	**B% PB%**	S1, S2, D	(S1) ÷ (S2) → quotient (D) remainder (DT9015 for FP3 or DT90015 for FP10SH)	**7**	**A**	**A**
F53 P53	**8-digit BCD data division**	**DB% PDB%**	S1, S2, D	(S1+1, S1) ÷ (S2+1, S2) → quotient (D+1, D) remainder (DT9016, DT9015 for FP3 or DT90016, DT90015 for FP10SH)	**11**	**A**	**A**
F55 P55	**4-digit BCD data increment**	**B+1 PB+1**	D	(D) + 1 → (D)	**3**	**A**	**A**
F56 P56	**8-digit BCD data increment**	**DB+1 PDB+1**	D	(D+1, D) + 1 → (D+1, D)	**3**	**A**	**A**
F57 P57	**4-digit BCD data decrement**	**B−1 PB−1**	D	(D) − 1 → (D)	**3**	**A**	**A**
F58 P58	**8-digit BCD data decrement**	**DB−1 PDB−1**	D	(D+1, D) − 1 → (D+1, D)	**3**	**A**	**A**
Data compare instructions							
F60 P60	**16-bit data compare**	**CMP PCMP**	S1, S2	(S1) > (S2) → R900A: ON (S1) = (S2) → R900B: ON (S1) < (S2) → R900C: ON	**5**	**A**	**A**
F61 P61	**32-bit data compare**	**DCMP PDCMP**	S1, S2	(S1+1, S1) > (S2+1, S2) → R900A: ON (S1+1, S1) = (S2+1, S2) → R900B: ON (S1+1, S1) < (S2+1, S2) → R900C: ON	**9**	**A**	**A**
F62 P62	**16-bit data band compare**	**WIN PWIN**	S1, S2, S3	(S1) > (S3) → R900A: ON (S2) ≦ (S1) ≦ (S3) → R900B: ON (S1) < (S2) → R900C: ON	**7**	**A**	**A**

☞ **Note**

A: Available

Number	Name	Boolean	Operand	Description	Steps	Availability	
						FP3	FP10SH
F63 P63	**32-bit data band compare**	**DWIN PDWIN**	S1, S2, S3	(S1+1, S1) > (S3+1, S3) → R900A: ON (S2+1, S2) ≦ (S1+1, S1) ≦ (S3 + 1, S3) → R900B: ON (S1+1, S1) < (S2+1, S2) → R900C: ON	**13**	**A**	**A**
F64 P64	**Block data compare**	**BCMP PBCMP**	S1, S2, S3	Compares the two blocks begining with “S2” and “S3” to see if they are equal.	**7**	**A (* Note 1)**	**A**
Logic operation instructions							
F65 P65	**16-bit data AND**	**WAN PWAN**	S1, S2, D	(S1) ∧ (S2) → (D)	**7**	**A**	**A**
F66 P66	**16-bit data OR**	**WOR PWOR**	S1, S2, D	(S1) ∨ (S2) → (D)	**7**	**A**	**A**
F67 P67	**16-bit data exclusive OR**	**XOR PXOR**	S1, S2, D	{(S1) ∧ ($\overline{S2}$)} ∨ {($\overline{S1}$) ∧ (S2)} → (D)	**7**	**A**	**A**
F68 P68	**16-bit data exclusive NOR**	**XNR PXNR**	S1, S2, D	{(S1) ∧ (S2)} ∨ {($\overline{S1}$) ∧ ($\overline{S2}$)} → (D)	**7**	**A**	**A**
F69 P69	**16-bit data unite**	**WUNI PWUNI**	S1, S2, S3, D	([S1] ∧ [S3]) ∨ ([S2] ∧ [$\overline{S3}$]) → (D) When (S3) is H0, (S2) → (D) When (S3) is HFFFF, (S1) → (D)	**9**	**N/A**	**A (* Note 2)**
Data conversion instructions							
F70 P70	**Block check code calculation**	**BCC PBCC**	S1, S2, S3, D	Creates the code for checking the data specified by “S2” and “S3” and stores it in “D.” The calculation method is specified by “S1.”	**9**	**A (* Note 3)**	**A**

☞ Notes

- **A: Available, N/A: Not available**
- **(*1): The instruction for FP3 is available for FP3 CPU Ver.4.0 or later. This instruction for FP3 should be input using NPST–GR Ver.2.3 or later and FP programmer II (AFP1114V2).**
- **(*2): The instruction for FP10SH should be input using NPST–GR Ver.4.0 or later.**
- **(*3): The instruction for FP3 is available for FP3 CPU Ver.3.1 or later.**

G.2 Table of High-Level Instructions

Number	Name	Boolean	Operand	Description	Steps	Availability	
						FP3	FP10SH
F71 P71	**Hexadecimal data → ASCII code**	**HEXA PHEXA**	S1, S2, D	Converts the hexadecimal data specified by “S1” and “S2” to ASCII code and stores it in “D.” Example: HABCD → H 42 41 44 43 B A D C	**7**	**A** **(* Note 1)**	**A**
F72 P72	**ASCII code → Hexadecimal data**	**AHEX PAHEX**	S1, S2, D	Converts the ASCII code specified by “S1” and “S2” to hexadecimal data and stores it in “D.” Example: H 44 43 42 41 → HABCD D C B A	**7**	**A** **(* Note 1)**	**A**
F73 P73	**4-digit BCD data → ASCII code**	**BCDA PBCDA**	S1, S2, D	Converts the four digits of BCD data specified by “S1” and “S2” to ASCII code and stores it in “D.” Example: H1234 → H 32 31 34 33 2 1 4 3	**7**	**A** **(* Note 1)**	**A**
F74 P74	**ASCII code → 4-digit BCD data**	**ABCD PABCD**	S1, S2, D	Converts the ASCII code specified by “S1” and “S2” to four digits of BCD data and stores it in “D.” Example: H 34 33 32 31 → H3412 4 3 2 1	**9**	**A** **(* Note 1)**	**A**
F75 P75	**16-bit binary data → ASCII code**	**BINA PBINA**	S1, S2, D	Converts the 16 bits of binary data specified by “S1” to ASCII code and stores it in “D” (area of “S2” bytes). Example: K–100 → H 30 30 31 2D 20 20 0 0 1 –	**7**	**A** **(* Note 1)**	**A**

☞ **Notes**

- **A: Available**
- **(*1): The instruction for FP3 is available for FP3 CPU Ver.3.1 or later.**

Number	Name	Boolean	Operand	Description	Steps	Availability	
						FP3	FP10SH
F76 P76	**ASCII code → 16-bit binary data**	**ABIN PABIN**	S1, S2, D	Converts the ASCII code specified by “S1” and “S2” to 16 bits of binary data and stores it in “D.” Example: H 30 30 31 2D 20 20→ 0 0 1 – K–100	**7**	**A** **(* Note 1)**	**A**
F77 P77	**32-bit binary data → ASCII code**	**DBIA PDBIA**	S1, S2, D	Converts the 32 bits of binary data (S1+1, S1) to ASCII code and stores it in (D+1, D).	**11**	**A** **(* Note 1)**	**A**
F78 P78	**ASCII code → 32-bit binary data**	**DABI PDABI**	S1, S2, D	Converts the ASCII code specified by “S1” and “S2” to 32 bits of binary data and stores it in (D+1, D).	**11**	**A** **(* Note 1)**	**A**
F80 P80	**16-bit binary data → 4-digit BCD data**	**BCD PBCD**	S, D	Converts the 16 bits of binary data specified by “S” to four digits of BCD data and stores it in “D.” Example: K100 → H100	**5**	**A**	**A**
F81 P81	**4-digit BCD data → 16-bit binary data**	**BIN PBIN**	S, D	Converts the four digits of BCD data specified by “S” to 16 bits of binary data and stores it in “D.” Example: H100 → K100	**5**	**A**	**A**
F82 P82	**32-bit binary data → 8-digit BCD data**	**DBCD PDBCD**	S, D	Converts the 32 bits of binary data specified by (S+1, S) to eight digits of BCD data and stores it in (D+1, D).	**7**	**A**	**A**
F83 P83	**8-digit BCD data → 32-bit binary data**	**DBIN PDBIN**	S, D	Converts the eight digits of BCD data specified by (S+1, S) to 32 bits of binary data and stores it in (D+1, D).	**7**	**A**	**A**
F84 P84	**16-bit data invert (complement of 1)**	**INV PINV**	D	Inverts each bit of data of “D.”	**3**	**A**	**A**

☞ **Notes**

- **A: Available**
- **(*1): The instruction for FP3 is available for FP3 CPU Ver.3.1 or later.**

G.2 Table of High-Level Instructions

Number	Name	Boolean	Operand	Description	Steps	Availability	
						FP3	FP10SH
F85 P85	**16-bit data complement of 2**	**NEG PNEG**	D	Inverts each bit of data of “D” and adds 1 (inverts the sign).	**3**	**A**	**A**
F86 P86	**32-bit data complement of 2**	**DNEG PDNEG**	D	Inverts each bit of data of (D+1, D) and adds 1 (inverts the sign).	**3**	**A**	**A**
F87 P87	**16-bit data absolute**	**ABS PABS**	D	Gives the absolute value of the data of “D.”	**3**	**A**	**A**
F88 P88	**32-bit data absolute**	**DABS PDABS**	D	Gives the absolute value of the data of (D+1, D).	**3**	**A**	**A**
F89 P89	**16-bit data sign extension**	**EXT PEXT**	D	Extends the 16 bits of data in “D” to 32 bits in (D+1, D).	**3**	**A**	**A**
F90 P90	**Decode**	**DECO PDECO**	S, n, D	Decodes part of the data of “S” and stores it in “D.” The part is specified by “n.”	**7**	**A**	**A**
F91 P91	**7-segment decode**	**SEGT PSEGT**	S, D	Converts the data of “S” for use in a 7-segment display and stores it in (D+1, D).	**5**	**A**	**A**
F92 P92	**Encode**	**ENCO PENCO**	S, n, D	Encodes part of the data of “S” and stores it in “D.” The part is specified by “n.”	**7**	**A**	**A**
F93 P93	**16-bit data combine**	**UNIT PUNIT**	S, n, D	The least significant digit of each of the “n” words of data begining at “S” are stored (united) in order in “D.”	**7**	**A**	**A**
F94 P94	**16-bit data distribute**	**DIST PDIST**	S, n, D	Each of the digits of the data of “S” are stored in (distributed to) the least significant digits of the areas beginning at “D.”	**7**	**A**	**A**
F95 P95	**Character → ASCII code**	**ASC PASC**	S, D	Twelve characters of the character constants of “S” are converted to ASCII code and stored in “D” to “D+5.”	**15**	**A**	**A**

☞ **Note**

A: Available

Number	Name	Boolean	Operand	Description	Steps	Availability	
						FP3	FP10SH
F96 P96	**16-bit table data search**	**SRC PSRC**	S1, S2, S3	The data of “S1” is searched for in the areas in the range “S2” to “S3” and the result is stored in DT9037 and DT9038 for FP3 and DT90037 and DT90038 for FP10SH.	**7**	**A**	**A**
F97 P97	**32-bit table data search**	**DSRC PDSRC**	S1, S2, S3, S4	The data of (S1+1, S1) is searched for in the 32-bit data designated by “S3”, beginning from “S2”, and the result is stored in DT90037 and DT90038.	**11**	**N/A**	**A (* Note 1)**
Data shift instructions							
F98 P98	**Data table shift-out and compress**	**CMPR PCMPR**	D1, D2, D3	Transfer “D2” to “D3.” Any parts of the data between “D1” and “D2” that are 0 are compressed, and shifted in order toward “D2.”	**7**	**A (* Note 2)**	**A**
F99 P99	**Data table shift-in and compress**	**CMPW PCMPW**	S, D1, D2	Transfer “S” to “D1”. Any parts of the data between “D1” and “D2” that are 0 are compressed, and shifted in order toward “D2.”	**7**	**A (* Note 2)**	**A**
F100 P100	**Right shift of multiple bits (n bits) in a 16-bit data**	**SHR PSHR**	D, n	Shifts the “n” bits of “D” to the right.	**5**	**A**	**A**
F101 P101	**Left shift of multiple bits (n bits) in a 16-bit data**	**SHL PSHL**	D, n	Shifts the “n” bits of “D” to the left.	**5**	**A**	**A**
F102 P102	**Right shift of n bits in a 32-bit data**	**DSHR PDSHR**	D, n	Shifts the “n” bits of the 32-bit data area specified by (D+1, D) to the right.	**5**	**N/A**	**A (* Note 1)**

☞ **Notes**

- **A: Available, N/A: Not available**
- **(*1): The instruction for FP10SH should be input using NPST–GR Ver.4.0 or later.**
- **(*2): The instruction for FP3 is available for FP3 CPU Ver.3.1 or later.**

G.2 Table of High-Level Instructions

Number	Name	Boolean	Operand	Description	Steps	Availability	
						FP3	FP10SH
F103 P103	**Left shift of n bits in a 32-bit data**	**DSHL PDSHL**	D, n	Shifts the “n” bits of the 32-bit data area specified by (D+1, D) to the left.	**5**	**N/A**	**A (* Note 1)**
F105 P105	**Right shift of one hexadecimal digit (4-bit)**	**BSR PBSR**	D	Shifts the one digit of data of “D” to the right.	**3**	**A**	**A**
F106 P106	**Left shift of one hexadecimal digit (4-bit)**	**BSL PBSL**	D	Shifts the one digit of data of “D” to the left.	**3**	**A**	**A**
F108 P108	**Right shift of multiple bits (n bits)**	**BITR PBITR**	D1, D2, n	Shifts the “n” bits of data range by “D1” and “D2” to the right.	**7**	**N/A**	**A (* Note 1)**
F109 P109	**Left shift of multiple bits (n bits)**	**BITL PBITL**	D1, D2, n	Shifts the “n” bits of data range by “D1” and “D2” to the left.	**7**	**N/A**	**A (* Note 1)**
F110 P110	**Right shift of one word (16-bit)**	**WSHR PWSHR**	D1, D2	Shifts the one word of the areas by “D1” and “D2” to the right.	**5**	**A**	**A**
F111 P111	**Left shift of one word (16-bit)**	**WSHL PWSHL**	D1, D2	Shifts the one word of the areas by “D1” and “D2” to the left.	**5**	**A**	**A**
F112 P112	**Right shift of one hexadecimal digit (4-bit)**	**WBSR PWBSR**	D1, D2	Shifts the one digit of the areas by “D1” and “D2” to the right.	**5**	**A**	**A**
F113 P113	**Left shift of one hexadecimal digit (4-bit)**	**WBSL PWBSL**	D1, D2	Shifts the one digit of the areas by “D1” and “D2” to the left.	**5**	**A**	**A**
FIFO instructions							
F115 P115	**FIFO buffer define**	**FIFT PFIFT**	n, D	The “n” words beginning from “D” are defined in the buffer.	**5**	**A**	**A**
F116 P116	**Data read from FIFO buffer**	**FIFR PFIFR**	S, D	The oldest data beginning from “S” that was written to the buffer is read and stored in “D.”	**5**	**A**	**A**

☞ **Notes**

- **A: Available, N/A: Not available**
- **(*1): The instruction for FP10SH should be input using NPST–GR Ver.4.0 or later.**

Number	Name	Boolean	Operand	Description	Steps	Availability	
						FP3	FP10SH
F117 P117	**Data write into FIFO buffer**	**FIFW PFIFW**	S, D	The data of “S” is written to the buffer starting from “D.”	**5**	**A**	**A**
Basic function instructions							
F118	**UP/DOWN counter**	**UDC**	S, D	Counts up or down from the value preset in “S” and stores the elapsed value in “D.”	**5**	**A**	**A**
F119	**Left/right shift register**	**LRSR**	D1, D2	Shifts one bit to the left or right with the area between “D1” and “D2” as the register.	**5**	**A**	**A**
Data rotate instructions							
F120 P120	**16-bit data right rotate**	**ROR PROR**	D, n	Rotate the “n” bits in data of “D” to the right.	**5**	**A**	**A**
F121 P121	**16-bit data left rotate**	**ROL PROL**	D, n	Rotate the “n” bits in data of “D” to the left.	**5**	**A**	**A**
F122 P122	**16-bit data right rotate with carry flag (R9009) data**	**RCR PRCR**	D, n	Rotate the “n” bits in 17-bit area consisting of “D” plus the carry flag (R9009) data to the right.	**5**	**A**	**A**
F123 P123	**16-bit data left rotate with carry flag (R9009) data**	**RCL PRCL**	D, n	Rotate the “n” bits in 17-bit area consisting of “D” plus the carry flag (R9009) data to the left.	**5**	**A**	**A**
F125 P125	**32-bit data right rotate**	**DROR PDROR**	D, n	Rotate the number of bits specified by “n” of the double words data (32 bits) specified by (D+1, D) to the right.	**5**	**N/A**	**A (* Note 1)**
F126 P126	**32-bit data left rotate**	**DROL PDROL**	D, n	Rotate the number of bits specified by “n” of the double words data (32 bits) specified by (D+1, D) to the left.	**5**	**N/A**	**A (* Note 1)**

☞ **Notes**

- **A: Available, N/A: Not available**
- **(*1): The instruction for FP10SH should be input using NPST–GR Ver.4.0 or later.**

Number	Name	Boolean	Operand	Description	Steps	Availability	
						FP3	FP10SH
F127 P127	**32-bit data right rotate with carry flag (R9009) data**	**DRCR PDRCR**	D, n	Rotate the number of bits specified by “n” of the double words data (32 bits) specified by (D+1, D) to the right together with carry flag (R9009) data.	**5**	**N/A**	**A (* Note 1)**
F128 P128	**32-bit data left rotate with carry flag (R9009) data**	**DRCL PDRCL**	D, n	Rotate the number of bits specified by “n” of the double words data (32 bits) specified by (D+1, D) to the left together with carry flag (R9009) data.	**5**	**N/A**	**A (* Note 1)**
Bit manipulation instructions							
F130 P130	**16-bit data bit set**	**BTS PBTS**	D, n	Set the value of bit position “n” of the data of “D” to 1.	**5**	**A**	**A**
F131 P131	**16-bit data bit reset**	**BTR PBTR**	D, n	Set the value of bit position “n” of the data of “D” to 0.	**5**	**A**	**A**
F132 P132	**16-bit data bit invert**	**BTI PBTI**	D, n	Invert the value of bit position “n” of the data of “D.”	**5**	**A**	**A**
F133 P133	**16-bit data bit test**	**BTT PBTT**	D, n	Test the value of bit position “n” of the data of “D” and output the result to R900B.	**5**	**A**	**A**
F135 P135	**Number of ON (1) bits in 16-bit data**	**BCU PBCU**	S, D	Store the number of ON bits in the data of “S” in “D.”	**5**	**A**	**A**
F136 P136	**Number of ON (1) bits in 32-bit data**	**DBCU PDBCU**	S, D	Store the number of ON bits in the data of (S+1, S) in “D.”	**7**	**A**	**A**

☞ Notes

- **A: Available, N/A: Not available**
- **(*1): The instruction for FP10SH should be input using NPST−GR Ver.4.0 or later.**

Number	Name	Boolean	Operand	Description	Steps	Availability	
						FP3	FP10SH
Basic function instruction							
F137	**Auxiliary timer**	**STMR**	S, D	Turn ON the specified output **(* Note 1)** and R900D after 0.01 sec. × set value.	**5**	**A** (* Note 2)	**A**
Special instructions							
F138 P138	**Hours, minutes and seconds data to seconds data**	**HMSS PHMSS**	S, D	Converts the hour, minute and second data of (S+1, S) to seconds data, and the converted data is stored in (D+1, D).	**5**	**A** (* Note 3)	**A**
F139 P139	**Seconds data to hours, minutes and seconds data**	**SHMS PSHMS**	S, D	Converts the seconds data of (S+1, S) to hour, minute and second data, and the converted data is stored in (D+1, D).	**5**	**A** (* Note 3)	**A**
F140 P140	**Carry flag (R9009) set**	**STC PSTC**	—	Turns ON the carry flag (R9009).	**1**	**A**	**A**
F141 P141	**Carry flag (R9009) reset**	**CLC PCLC**	—	Turns OFF the carry flag (R9009).	**1**	**A**	**A**
F142 P142	**Watching dog timer update**	**WDT PWDT**	S	The time (allowable scan time for the system) of watching dog timer is changed to "S" × 0.1 (ms) only for that scan.	**3**	**N/A**	**A**
F143 P143	**Partial I/O update**	**IORF PIORF**	D1, D2	Updates the I/O from the number specified by "D1" to the number specified by "D2."	**5**	**A**	**A**

☞ Notes

- **A: Available, N/A: Not available**
- **(*1): In FP3/FP10SH CPU Ver.4.0 or later, an OT instruction can be entered after an auxiliary timer instruction. This instruction should be input using NPST–GR Ver.2.3 or later and FP programmer II (AFP1114V2).**
- **(*2): The instruction for FP3 is available for FP3 CPU Ver.3.1 or later.**
- **(*3): The instruction for FP3 is available for FP3 CPU Ver.4.0 or later.**

G.2 Table of High-Level Instructions

Number	Name	Boolean	Operand	Description	Steps	Availability	
						FP3	FP10SH
F144 P144	**Serial data communica-tion control**	**TRNS PTRNS**	S, n	The COM port receive flag (R9038) is set to OFF to enable reception. Beginning at “S”, “n” bytes of the data registers are sent from the COM port.	**5**	**N/A**	**A (* Note 1)**
F145 P145	**Data send**	**SEND PSEND**	S1, S2, D, N	Sends the data to another station in the network (MEWNET).	**9**	**A**	**A**
F146 P146	**Data receive**	**RECV PRECV**	S1, S2, N, D	Receives the data to another station in the network (MEWNET).	**9**	**A**	**A**
F147	**Printout**	**PR**	S, D	Converts the ASCII code data in the area starting with “S” for printing, and outputs it to the word external output relay WY specified by “D.”	**5**	**A**	**A**
F148 P148	**Self-diagnos-tic error set**	**ERR PERR**	n (n: K100 to K299)	Stores the self-diagnostic error number “n” in (DT9000 for FP3 or DT90000 for FP10SH), turns R9000 ON, and turns ON the ERROR LED.	**3**	**A (* Note 2)**	**A (* Note 2)**
F149 P149	**Message display**	**MSG PMSG**	S	Displays the character constant of “S” in the connected programming tool.	**13**	**A**	**A**
F150 P150	**Data read from intelligent unit**	**READ PREAD**	S1, S2, n, D	Reads the data from the intelligent unit.	**9**	**A**	**A**
F151 P151	**Data write into intelligent unit**	**WRT PWRT**	S1, S2, n, D	Writes the data into the intelligent unit.	**9**	**A**	**A**

☞ **Notes**

- **A: Available, N/A: Not available**
- **(*1): The instruction for FP10SH should be input using NPST–GR Ver.4.0 or later.**
- **(*2): In FP3/FP10SH CPU Ver.4.4 or later, a self-diagnosis error can be cleared by executing the instruction with K0 specified for n.**

Number	Name	Boolean	Operand	Description	Steps	Availability	
						FP3	FP10SH
F152 P152	**Data read from MEWNET-F slave station**	**RMRD PRMRD**	S1, S2, n, D	Reads the data from the intelligent unit at the MEWNET-F (remote I/O) slave station.	**9**	**A**	**A**
F153 P153	**Data write into MEWNET-F slave station**	**RMWT PRMWT**	S1, S2, n, D	Writes the data into the intelligent unit at the MEWNET-F (remote I/O) slave station.	**9**	**A**	**A**
F154 P154	**Machine language program call**	**MCAL PMCAL**	n	The machine language program is called.	**3**	**A**	**N/A**
F155 P155	**Sampling**	**SMPL PSMPL**	—	Starts sampling data.	**1**	**A**	**A**
F156 P156	**Sampling trigger**	**STRG PSTRG**	—	When the trigger of this instruction turns ON, the sampling trace stops.	**1**	**A**	**A**
F157 P157	**Time addition**	**CADD PCADD**	S1, S2, D	The time after (S2+1, S2) elapses from the time of (S1+2, S1+1, S1) is stored in (D+2, D+1, D).	**9**	**A**	**A**
F158 P158	**Time substruction**	**CSUB PCSUB**	S1, S2, D	The time that results from subtracting (S2+1, S2) from the time (S1+2, S1+1, S1) is stored in (D+2, D+1, D).	**9**	**A**	**A**
BIN arithmetic instruction							
F160 P160	**Double word (32-bit) data square root**	**DSQR PDSQR**	S, D	$\sqrt{(S)} \rightarrow (D)$	**7**	**A**	**A**
Basic function instruction							
F183	**Auxiliary timer (32-bit)**	**DSTM**	S, D	Turn ON the specified output and R900D after 0.01 sec. × set value.	**7**	**N/A**	**A (* Note 1)**

☞ **Notes**

- **A: Available, N/A: Not available**
- **(*1): The instruction for FP10SH is available for FP10SH CPU Ver.3.1 or later and this instruction for FP10SH should be input using NPST–GR Ver.4.0 or later.**

Number	Name	Boolean	Operand	Description	Steps	Availability	
						FP3	FP10SH
Data transfer instructions							
F190 P190	**Three 16-bit data move**	**MV3 PMV3**	S1, S2, S3, D	(S1) → (D), (S2) → (D+1), (S3) → (D+2)	**10**	**N/A**	**A (* Note 1)**
F191 P191	**Three 32-bit data move**	**DMV3 PDMV3**	S1, S2, S3, D	(S1+1, S1) → (D+1, D), (S2+1, S2) → (D+3, D+2), (S3+1, S3) → (D+5, D+4)	**16**	**N/A**	**A (* Note 1)**
Logic operation instructions							
F215 P215	**32-bit data AND**	**DAND PDAND**	S1, S2, D	(S1+1, S1) ∧ (S2+1, S2) → (D+1, D)	**12**	**N/A**	**A (* Note 1)**
F216 P216	**32-bit data OR**	**DOR PDOR**	S1, S2, D	(S1+1, S1) ∨ (S2+1, S2) → (D+1, D)	**12**	**N/A**	**A (* Note 1)**
F217 P217	**32-bit data XOR**	**DXOR PDXOR**	S1, S2, D	{(S1+1, S1) ∧ $\overline{(S2+1, S2)}$} ∨ {$\overline{(S1+1, S1)}$ ∧ (S2+1, S2)} → (D+1, D)	**12**	**N/A**	**A (* Note 1)**
F218 P218	**32-bit data XNR**	**DXNR PDXNR**	S1, S2, D	{(S1+1, S1) ∧ (S2+1, S2)} ∨ {$\overline{(S1+1, S1)}$ ∧ $\overline{(S2+1, S2)}$} → (D+1, D)	**12**	**N/A**	**A (* Note 1)**
F219 P219	**Double word (32-bit) data unites**	**DUNI PDUNI**	S1, S2, S3, D	{(S1+1, S1) ∧ (S3+1, S3)} ∨ {(S2+1, S2) ∧ $\overline{(S3+1, S3)}$} → (D+1, D)	**16**	**N/A**	**A (* Note 1)**
Data conversion instructions							
F235 P235	**16-bit binary data → Gray code conversion**	**GRY PGRY**	S, D	Converts the 16-bit binary data of “S” to gray codes, and the converted result is stored in the “D.”	**6**	**N/A**	**A (* Note 1)**
F236 P236	**32-bit binary data → Gray code conversion**	**DGRY PDGRY**	S, D	Converts the 32-bit binary data of (S+1, S) to gray code, and the converted data is stored in the (D+1, D).	**8**	**N/A**	**A (* Note 1)**
F237 P237	**16-bit gray code → binary data conversion**	**GBIN PGBIN**	S, D	Converts the gray codes of “S” to binary data, and the converted result is stored in the “D.”	**6**	**N/A**	**A (* Note 1)**

☞ Notes

- **A: Available, N/A: Not available**
- **(*1): The instruction for FP10SH should be input using NPST–GR Ver.4.0 or later.**

Number	Name	Boolean	Operand	Description	Steps	Availability	
						FP3	FP10SH
F238 P238	**32-bit gray code → binary data conversion**	**DGBIN PDGBIN**	S, D	Converts the gray code of (S+1, S) to binary data,and the converted result is stored in the (D+1, D).	**8**	**N/A**	**A (* Note 1)**
F240 P240	**Bit line to bit column conversion**	**COLM PCOLM**	S1, S2, D	The values of bits 0 to 15 of “S” are stored in bit “n” of (D to D+15).	**8**	**N/A**	**A (* Note 1)**
F241 P241	**Bit column to bit line conversion**	**LINE PLINE**	S1, S2, D	The values of bit “n” of (S to S+15) are stored in bits 0 to 15 of “D.”	**8**	**N/A**	**A (* Note 1)**
Integer type data processing instructions							
F270 P270	**Maximum value (word data (16-bit))**	**MAX PMAX**	S1, S2, D	Searches the maximum value in the word data table between the “S1” and “S2”, and stores it in the “D.” The address relative to “S1” is stored in “D+1.”	**8**	**N/A**	**A (* Note 1)**
F271 P271	**Maximum value (double word data (32-bit))**	**DMAX PDMAX**	S1, S2, D	Searches for the maximum value in the double word data table between the area selected with “S1” and “S2”, and stores it in the “D.” The address relative to “S1” is stored in “D+2.”	**8**	**N/A**	**A (* Note 1)**
F272 P272	**Minimum value (word data (16-bit))**	**MIN PMIN**	S1, S2, D	Searches for the minimum value in the word data table between the area selected with “S1” and “S2”, and stores it in the “D.” The address relative to “S1” is stored in “D+1.”	**8**	**N/A**	**A (* Note 1)**

☞ Notes

- **A: Available, N/A: Not available**
- **(*1): The instruction for FP10SH should be input using NPST–GR Ver.4.0 or later.**

Number	Name	Boolean	Operand	Description	Steps	Availability	
						FP3	FP10SH
F273 P273	**Minimum value (double word data (32-bit))**	**DMIN PDMIN**	S1, S2, D	Searches for the minimum value in the double word data table between the area selected with “S1” and “S2”, and stores it in the “D”. The address relative to “S1” is stored in “D+2.”	**8**	**N/A**	**A (* Note 1)**
F275 P275	**Total and mean values (word data (16-bit))**	**MEAN PMEAN**	S1, S2, D	The total value and the mean value of the word data with sign from the area selected with “S1” to the “S2” are obtained and stored in the “D.”	**8**	**N/A**	**A (* Note 1)**
F276 P276	**Total and mean values (double word data (32-bit))**	**DMEAN PDMEAN**	S1, S2, D	The total value and the mean value of the double word data with sign from the area selected with “S1” to “S2” are obtained and stored in the “D.”	**8**	**N/A**	**A (* Note 1)**
F277 P277	**Sort (word data (16-bit))**	**SORT PSORT**	S1, S2, S3	The word data with sign from the area specified by “S1” to “S2” are sorted in ascending order (the smallest word is first) or descending order (the largest word is first).	**8**	**N/A**	**A (* Note 1)**
F278 P278	**Sort (double word data (32-bit))**	**DSORT PDSORT**	S1, S2, S3	The double word data with sign from the area specified by “S1” to “S2” are sorted in ascending order (the smallest word is first) or descending order (the largest word is first).	**8**	**N/A**	**A (* Note 1)**
Integer type non-linear function instructions							
F285 P285	**Upper and lower limit control (16-bit data)**	**LIMT PLIMT**	S1, S2, S3, D	When S1 > S3, S1 → D When S2 < S3, S2 → D When S1 ≦ S3 ≦ S2, S3 → D	**10**	**N/A**	**A (* Note 1)**

☞ **Notes**

- **A: Available, N/A: Not available**
- **(*1): The instruction for FP10SH should be input using NPST–GR Ver.4.0 or later.**

Number	Name	Boolean	Operand	Description	Steps	Availability	
						FP3	FP10SH
F286 P286	**Upper and lower limit control (32-bit data)**	**DLIMT PDLIMT**	S1, S2, S3, D	When (S1+1, S1) > (S3+1, S3), (S1+1, S1) → (D+1, D) When (S2+1, S2) < (S3+1, S3), (S2+1, S2) → (D+1, D) When (S1+1, S1) ≦ (S3+1, S3) ≦ (S2+1, S2), (S3+1, S3) → (D+1, D)	**16**	**N/A**	**A** (* Note 1)
F287 P287	**Deadband control (16-bit data)**	**BAND PBAND**	S1, S2, S3, D	When S1 > S3, S3 – S1 → D When S2 < S3, S3 – S2 → D When S1 ≦ S3 ≦ S2, 0 → D	**10**	**N/A**	**A** (* Note 1)
F288 P288	**Deadband control (32-bit data)**	**DBAND PDBAND**	S1, S2, S3, D	When (S1+1, S1) > (S3+1, S3), (S3+1, S3) – (S1+1, S1) → (D+1, D) When (S2+1, S2) < (S3+1, S3), (S3+1, S3) – (S2+1, S2) → (D+1, D) When (S1+1, S1) ≦ (S3+1, S3) ≦ (S2+1, S2), 0 → (D+1, D)	**16**	**N/A**	**A** (* Note 1)
F289 P289	**Zone control (16-bit data)**	**ZONE PZONE**	S1, S2, S3, D	When S3 < 0, S3 + S1 → D When S3 = 0, 0 → D When S3 > 0, S3 + S2 → D	**10**	**N/A**	**A** (* Note 1)
F290 P290	**Zone control (32-bit data)**	**DZONE PDZONE**	S1, S2, S3, D	When (S3+1, S3) < 0, (S3+1, S3) + (S1+1, S1) → (D+1, D) When (S3+1, S3) = 0, 0 → (D+1, D) When (S3+1, S3) > 0, (S3+1, S3) + (S2+1, S2) → (D+1, D)	**16**	**N/A**	**A** (* Note 1)

☞ **Notes**

- **A: Available, N/A: Not available**
- **(*1): The instruction for FP10SH should be input using NPST–GR Ver.4.0 or later.**

G.2 Table of High-Level Instructions

Number	Name	Boolean	Operand	Description	Steps	Availability	
						FP3	FP10SH
BCD type real number operation instructions							
F300 P300	**BCD type sine operation**	**BSIN PBSIN**	S, D	SIN (S+1, S) → (D+1, D)	**6**	**N/A**	**A (* Note 1)**
F301 P301	**BCD type cosine operation**	**BCOS PBCOS**	S, D	COS (S+1, S) → (D+1, D)	**6**	**N/A**	**A (* Note 1)**
F302 P302	**BCD type tangent operation**	**BTAN PBTAN**	S, D	TAN (S+1, S) → (D+1, D)	**6**	**N/A**	**A (* Note 1)**
F303 P303	**BCD type arcsine operation**	**BASIN PBASIN**	S, D	SIN^{-1} (S+1, S) → (D+1, D)	**6**	**N/A**	**A (* Note 1)**
F304 P304	**BCD type arccosine operation**	**BACOS PBACOS**	S, D	COS^{-1} (S+1, S) → (D+1, D)	**6**	**N/A**	**A (* Note 1)**
F305 P305	**BCD type arctangent operation**	**BATAN PBATAN**	S, D	TAN^{-1} (S+1, S) → (D+1, D)	**6**	**N/A**	**A (* Note 1)**
Floating-point type real number operation instructions							
F309 P309	**Floating-point type real data move**	**FMV PFMV**	S, D	(S+1, S) → (D+1, D)	**8**	**N/A**	**A (* Note 1)**
F310 P310	**Floating-point type real data addition**	**F+ PF+**	S1, S2, D	(S1+1, S1) + (S2+1, S2)→ (D+1, D)	**14**	**N/A**	**A (* Note 1)**
F311 P311	**Floating-point type real data subtraction**	**F– PF–**	S1, S2, D	(S1+1, S1) – (S2+1, S2)→ (D+1, D)	**14**	**N/A**	**A (* Note 1)**
F312 P312	**Floating-point type real data multiplication**	**F* PF***	S1, S2, D	(S1+1, S1) × (S2+1, S2)→ (D+1, D)	**14**	**N/A**	**A (* Note 1)**
F313 P313	**Floating-point type real data division**	**F% PF%**	S1, S2, D	(S1+1, S1) ÷ (S2+1, S2)→ (D+1, D)	**14**	**N/A**	**A (* Note 1)**
F314 P314	**Floating-point type real data sine operation**	**SIN PSIN**	S, D	SIN (S+1, S) → (D+1, D)	**10**	**N/A**	**A (* Note 1)**

☞ **Notes**

- **A: Available, N/A: Not available**
- **(*1): The instruction for FP10SH should be input using NPST–GR Ver.4.0 or later.**

Number	Name	Boolean	Operand	Description	Steps	Availability	
						FP3	FP10SH
F315 P315	**Floating-point type real data cosine operation**	**COS PCOS**	S, D	COS (S+1, S) → (D+1, D)	**10**	**N/A**	**A (* Note 1)**
F316 P316	**Floating-point type real data tangent operation**	**TAN PTAN**	S, D	TAN (S+1, S) → (D+1, D)	**10**	**N/A**	**A (* Note 1)**
F317 P317	**Floating-point type real data arcsine operation**	**ASIN PASIN**	S, D	SIN^{-1} (S+1, S) → (D+1, D)	**10**	**N/A**	**A (* Note 1)**
F318 P318	**Floating-point type real data arccosine operation**	**ACOS PACOS**	S, D	COS^{-1} (S+1, S) → (D+1, D)	**10**	**N/A**	**A (* Note 1)**
F319 P319	**Floating-point type real data arctangent operation**	**ATAN PATAN**	S, D	TAN^{-1} (S+1, S) → (D+1, D)	**10**	**N/A**	**A (* Note 1)**
F320 P320	**Floating-point type real data natural logarithm**	**LN PLN**	S, D	LN (S+1, S) → (D+1, D)	**10**	**N/A**	**A (* Note 1)**
F321 P321	**Floating-point type real data exponent**	**EXP PEXP**	S, D	EXP (S+1, S) → (D+1, D)	**10**	**N/A**	**A (* Note 1)**
F322 P322	**Floating-point type real data logarithm**	**LOG PLOG**	S, D	LOG (S+1, S) → (D+1, D)	**10**	**N/A**	**A (* Note 1)**
F323 P323	**Floating-point type real data power**	**PWR PPWR**	S1, S2, D	(S1+1, S1) ^ (S2+1, S2) → (D+1, D)	**14**	**N/A**	**A (* Note 1)**
F324 P324	**Floating-point type real data square root**	**FSQR PFSQR**	S, D	$\sqrt{(S+1, S)}$ → (D+1, D)	**10**	**N/A**	**A (* Note 1)**

☞ **Notes**

- **A: Available, N/A: Not available**
- **(*1): The instruction for FP10SH should be input using NPST–GR Ver.4.0 or later.**

Number	Name	Boolean	Operand	Description	Steps	Availability	
						FP3	FP10SH
F325 P325	**16-bit integer data to floating-point type real data conversion**	**FLT PFLT**	S, D	Converts the 16-bit integer data with sign specified by “S” to real number data, and the converted data is stored in “D.”	**6**	**N/A**	**A (* Note 1)**
F326 P326	**32-bit integer data to floating-point type real data conversion**	**DFLT PDFLT**	S, D	Converts the 32-bit integer data with sign specified by (S+1, S) to real number data, and the converted data is stored in (D+1, D).	**8**	**N/A**	**A (* Note 1)**
F327 P327	**Floating-point type real data to 16-bit integer conversion (the largest integer not exceeding the floating-point type real data)**	**INT PINT**	S, D	Converts real number data specified by (S+1, S) to the 16-bit integer data with sign (the largest integer not exceeding the floating-point data), and the converted data is stored in “D.”	**8**	**N/A**	**A (* Note 1)**
F328 P328	**Floating-point type real data to 32-bit integer conversion (the largest integer not exceeding the floating-point type real data)**	**DINT PDINT**	S, D	Converts real number data specified by (S+1, S) to the 32-bit integer data with sign (the largest integer not exceeding the floating-point data), and the converted data is stored in (D+1, D).	**8**	**N/A**	**A (* Note 1)**
F329 P329	**Floating-point type real data to 16-bit integer conversion (rounding the first decimal point down to integer)**	**FIX PFIX**	S, D	Converts real number data specified by (S+1, S) to the 16-bit integer data with sign (rounding the first decimal point down), and the converted data is stored in “D.”	**8**	**N/A**	**A (* Note 1)**

☞ **Notes**

- **A: Available, N/A: Not available**
- **(*1): The instruction for FP10SH should be input using NPST–GR Ver.4.0 or later.**

Number	Name	Boolean	Operand	Description	Steps	Availability	
						FP3	FP10SH
F330 P330	**Floating-point type real data to 32-bit integer conversion (rounding the first decimal point down to integer)**	**DFIX PDFIX**	S, D	Converts real number data specified by (S+1, S) to the 32-bit integer data with sign (rounding the first decimal point down), and the converted data is stored in (D+1, D).	**8**	**N/A**	**A (* Note 1)**
F331 P331	**Floating-point type real data to 16-bit integer conversion (rounding the first decimal point off to integer)**	**ROFF PROFF**	S, D	Converts real number data specified by (S+1, S) to the 16-bit integer data with sign (rounding the first decimal point off), and the converted data is stored in “D.”	**8**	**N/A**	**A (* Note 1)**
F332 P332	**Floating-point type real data to 32-bit integer conversion (rounding the first decimal point off to integer)**	**DROFF PDROFF**	S, D	Converts real number data specified by (S+1, S) to the 32-bit integer data with sign(rounding the first decimal point off), and the converted data is stored in (D+1, D).	**8**	**N/A**	**A (* Note 1)**
F333 P333	**Floating-point type real data rounding the first decimal point down**	**FINT PFINT**	S, D	The decimal part of the real number data specified in (S+1, S) is rounded down, and the result is stored in (D+1, D).	**8**	**N/A**	**A (* Note 1)**
F334 P334	**Floating-point type real data rounding the first decimal point off**	**FRINT PFRINT**	S, D	The decimal part of the real number data stored in (S+1, S) is rounded off, and the result is stored in (D+1, D).	**8**	**N/A**	**A (* Note 1)**
F335 P335	**Floating-point type real data sign changes**	**F+/– PF+/–**	S, D	The real number data stored in (S+1, S) is changed the sign, and the result is stored in (D+1, D).	**8**	**N/A**	**A (* Note 1)**

☞ **Notes**

- **A: Available, N/A: Not available**
- **(*1): The instruction for FP10SH should be input using NPST–GR Ver.4.0 or later.**

Number	Name	Boolean	Operand	Description	Steps	Availability	
						FP3	FP10SH
F336 P336	**Floating-point type real data absolute**	**FABS PFABS**	S, D	Takes the absolute value of real number data specified by (S+1, S), and the result (absolute value) is stored in (D+1, D).	**8**	**N/A**	**A (* Note 1)**
F337 P337	**Floating-point type real data degree → radian**	**RAD PRAD**	S, D	The data in degrees of an angle specified in (S+1, S) is converted to radians (real number data), and the result is stored in (D+1, D).	**8**	**N/A**	**A (* Note 1)**
F338 P338	**Floating-point type real data radian → degree**	**DEG PDEG**	S, D	The angle data in radians (real number data) specified in (S+1, S) is converted to angle data in degrees, and the result is stored in (D+1, D).	**8**	**N/A**	**A (* Note 1)**
Floating-point type real number data processing instructions							
F345 P345	**Floating-point type real data compare**	**FCMP PFCMP**	S1, S2	(S1+1, S1) > (S2+1, S2) → R900A: ON (S1+1, S1) = (S2+1, S2) → R900B: ON (S1+1, S1) < (S2+1, S2) → R900C: ON	**10**	**N/A**	**A (* Note 1)**
F346 P346	**Floating-point type real data band compare**	**FWIN PFWIN**	S1, S2, S3	(S1+1, S1) > (S3+1, S3) → R900A: ON (S2+1, S2) ≦ (S1+1, S1) ≦ (S3+1,S3) → R900B: ON (S1+1, S1) < (S2+1, S2) → R900C: ON	**14**	**N/A**	**A (* Note 1)**

☞ **Notes**

- **A: Available, N/A: Not available**
- **(*1): The instruction for FP10SH should be input using NPST−GR Ver.4.0 or later.**

Number	Name	Boolean	Operand	Description	Steps	Availability	
						FP3	FP10SH
F347 P347	**Floating-point type real data upper and lower limit control**	**FLIMT PFLIMT**	S1, S2, S3, D	When (S1+1, S1) > (S3+1, S3), (S1+1, S1) → (D+1, D) When (S2+1, S2) < (S3+1, S3), (S2+1, S2) → (D+1, D) When (S1+1, S1) ≦ (S3+1, S3) ≦ (S2+1, S2), (S3+1, S3) → (D+1, D)	**17**	**N/A**	**A (* Note 1)**
F348 P348	**Floating-point type real data deadband control**	**FBAND PFBAND**	S1, S2, S3, D	When (S1+1, S1) > (S3+1, S3), (S3+1, S3) – (S1+1, S1) → (D+1, D) When (S2+1, S2) < (S3+1, S3), (S3+1, S3) – (S2+1, S2) → (D+1, D) When (S1+1, S1) ≦ (S3+1, S3) ≦ (S2+1, S2), 0.0 → (D+1, D)	**17**	**N/A**	**A (* Note 1)**
F349 P349	**Floating-point type real data zone control**	**FZONE PFZONE**	S1, S2, S3, D	When (S3+1, S3) < 0.0, (S3+1, S3) + (S1+1, S1) → (D+1, D) When (S3+1, S3) = 0.0, 0.0 → (D+1, D) When (S3+1, S3) > 0.0, (S3+1, S3) + (S2+1, S2) → (D+1, D)	**17**	**N/A**	**A (* Note 1)**
F350 P350	**Floating-point type real data maximum value**	**FMAX PFMAX**	S1, S2, D	Searches the maximum value in the real number data table between the area selected with “S1” and “S2”, and stores it in the (D+1, D). The address relative to “S1” is stored in (D+2).	**8**	**N/A**	**A (* Note 1)**

☞ Notes

- **A: Available, N/A: Not available**
- **(*1): The instruction for FP10SH should be input using NPST–GR Ver.4.0 or later.**

Number	Name	Boolean	Operand	Description	Steps	Availability	
						FP3	FP10SH
F351 P351	**Floating-point type real data minimum value**	**FMIN PFMIN**	S1, S2, D	Searches the minimum value in the real number data table between the area selected with “S1” and “S2”, and stores it in the (D+1, D). The address relative to “S1” is stored in (D+2).	**8**	**N/A**	**A (* Note 1)**
F352 P352	**Floating-point type real data total and mean values**	**FMEAN PFMEAN**	S1, S2, D	The total value and the mean value of the real number data from the area selected with “S1” to “S2” are obtained. The total value is stored in the (D+1, D) and the mean value is stored in the (D+3, D+2).	**8**	**N/A**	**A (* Note 1)**
F353 P353	**Floating-point type real data sort**	**FSORT PFSORT**	S1, S2, D	The real number data from the area specified by “S1” to “S2” are sorted in ascending order (the smallest word is first) or descending order (the largest word is first).	**8**	**N/A**	**A (* Note 1)**
Time series processing instruction							
F355 P355	**PID processing**	**PID PPID**	S	PID processing is performed depending on the control value (mode and parameter) specified by (S to S+2) and (S+4 to S+10), and the result is stored in the (S+3).	**4**	**N/A**	**A (* Note 1)**

☞ **Notes**

- **A: Available, N/A: Not available**
- **(*1): The instruction for FP10SH should be input using NPST–GR Ver.4.0 or later.**

Number	Name	Boolean	Operand	Description	Steps	Availability	
						FP3	FP10SH
Compare instructions							
F373 P373	**16-bit data revision detection**	**DTR PDTR**	S, D	If the data in the 16-bit area specified by “S” has changed since the previous execution, internal relay R9009 (carry flag) will turn ON. “D” is used to store the data of the previous execution.	**6**	**N/A**	**A (* Note 1)**
F374 P374	**32-bit data revision detection**	**DDTR PDDTR**	S, D	If the data in the 32-bit area specified by (S+1, S) has changed since the previous execution, internal relay R9009 (carry flag) will turn ON. (D+1, D) is used to store the data of the previous execution.	**6**	**N/A**	**A (* Note 1)**
Index register bank processing instructions							
F410 P410	**Index register bank change over**	**SETB PSETB**	S	Setting the index register (I0 to ID) bank.	**4**	**N/A**	**A (* Note 1)**
F411 P411	**Changing the index register bank**	**CHGB PCHGB**	S	Index register (I0 to ID) bank change over with remembering preceding bank.	**4**	**N/A**	**A (* Note 1)**
F412 P412	**Restoring the index register bank**	**POPB PPOPB**	—	Changes index register (I0 to ID) bank to the bank before **F411 (CHGB)**/**P411 (PCHGB)** instruction.	**2**	**N/A**	**A**

☞ Notes

- **A: Available, N/A: Not available**
- **(*1): The instruction for FP10SH should be input using NPST–GR Ver.4.0 or later.**

Appendix H

Table of Binary/Hexadecimal/BCD Expressions

Decimal	Hexadecimal	Binary	BCD code
0	0000	00000000 00000000	0000 0000 0000 0000
1	0001	00000000 00000001	0000 0000 0000 0001
2	0002	00000000 00000010	0000 0000 0000 0010
3	0003	00000000 00000011	0000 0000 0000 0011
4	0004	00000000 00000100	0000 0000 0000 0100
5	0005	00000000 00000101	0000 0000 0000 0101
6	0006	00000000 00000110	0000 0000 0000 0110
7	0007	00000000 00000111	0000 0000 0000 0111
8	0008	00000000 00001000	0000 0000 0000 1000
9	0009	00000000 00001001	0000 0000 0000 1001
10	000A	00000000 00001010	0000 0000 0001 0000
11	000B	00000000 00001011	0000 0000 0001 0001
12	000C	00000000 00001100	0000 0000 0001 0010
13	000D	00000000 00001101	0000 0000 0001 0011
14	000E	00000000 00001110	0000 0000 0001 0100
15	000F	00000000 00001111	0000 0000 0001 0101
16	0010	00000000 00010000	0000 0000 0001 0110
17	0011	00000000 00010001	0000 0000 0001 0111
18	0012	00000000 00010010	0000 0000 0001 1000
19	0013	00000000 00010011	0000 0000 0001 1001
20	0014	00000000 00010100	0000 0000 0010 0000
21	0015	00000000 00010101	0000 0000 0010 0001
22	0016	00000000 00010110	0000 0000 0010 0010
23	0017	00000000 00010111	0000 0000 0010 0011
24	0018	00000000 00011000	0000 0000 0010 0100
25	0019	00000000 00011001	0000 0000 0010 0101
26	001A	00000000 00011010	0000 0000 0010 0110
27	001B	00000000 00011011	0000 0000 0010 0111
28	001C	00000000 00011100	0000 0000 0010 1000
29	001D	00000000 00011101	0000 0000 0010 1001
30	001E	00000000 00011110	0000 0000 0011 0000
31	001F	00000000 00011111	0000 0000 0011 0001
⋮	⋮	⋮	⋮
63	003F	00000000 00111111	0000 0000 0110 0011
⋮	⋮	⋮	⋮
255	00FF	00000000 11111111	0000 0010 0101 0101
⋮	⋮	⋮	⋮
9999	270F	00100111 00001111	1001 1001 1001 1001

Appendix I

ASCII Codes

							b_6	0	0	0	0	1	1	1	1
							b_5	0	0	1	1	0	0	1	1
							b_4	0	1	0	1	0	1	0	1
b_6	b_5	b_4	b_3	b_2	b_1	b_0	ASCII HEX code	Most significant digit							
								0	1	2	3	4	5	6	7
			0	0	0	0	0	NUL	DEL	SPACE	0	@	P	`	p
			0	0	0	1	1	SOH	DC_1	!	1	A	Q	a	q
			0	0	1	0	2	STX	DC_2	〃	2	B	R	b	r
			0	0	1	1	3	ETX	DC_3	#	3	C	S	c	s
			0	1	0	0	4	EOT	DC_4	$	4	D	T	d	t
			0	1	0	1	5	ENQ	NAK	%	5	E	U	e	u
			0	1	1	0	6	ACK	SYN	&	6	F	V	f	v
			0	1	1	1	7	BEL	ETB	’	7	G	W	g	w
			1	0	0	0	8	BS	CAN	(	8	H	X	h	x
			1	0	0	1	9	HT	EM	)	9	I	Y	i	y
			1	0	1	0	A	LF	SUB	＊	:	J	Z	j	z
			1	0	1	1	B	VT	ESC	+	;	K	[	k	{
			1	1	0	0	C	FF	FS	,	<	L	¥	l	|
			1	1	0	1	D	CR	GS	–	=	M	]	m	}
			1	1	1	0	E	SO	RS	.	>	N	^	n	～
			1	1	1	1	F	SI	US	／	?	O	_	o	DEL

Least significant digit

Index

S

T

W

Record of changes

ACG No.	Date	Description of Changes
ACG−M0080−1	SEPT. 1997	First edition
ARCT1F300E/ ACG−M300E	FEB. 1999	2nd edition Newly addition of ROM/RAM memory information Newly addition of IC memory card information Size change (from A4 to B5)
ARCT1F300E−1/ ACG−M300E−1	SEPT. 2006	3rd edition

These materials are printed on ECF pulp.
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